

THE ACCORDION IMAGER: an Ultra High Density Frame Transfer CCD.

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ABSTRACT

A charge-coupled device image sensor with an ultra high density matrix of photo-sensitive elements is described. The development of a new storage and read-out mechanism and the combination of CCD- and CMOS-technology on a single chip, have led to the new device, called "the accordion imager".

INTRODUCTION

For solid-state imagers, such as CCD's, resolution and chip size are two contradictory properties. Increasing the number of pixels, without changing the critical dimensions of the device lay-out, is always at the expense of silicon area and yield. This paper describes the application of a new clocking method to a frame-transfer CCD-imager: the "ACCORDION CCD". With this type of CCD the number of pixels in the vertical direction of the classical four-phase image sensing device can be doubled without any increase in chip size, or the other way around: without changing the pixel number, the chip size can be halved. We used this principle in an imager with 588 interlaced lines with 604 pixels on each line, fully compatible with the PAL television standard. The consumed silicon area is only 38.22 mm².

THE ACCORDION READ-OUT MECHANISM

A cross-section of a classical four-phase frame-transfer CCD-imager is shown in figure 1. Part of the image section during the integration of an odd field with the corresponding potential is depicted in fig. 1a. To operate the CCD-imager in an interlaced mode, the potential profile as shown in fig. 1b is used during the even field integration. Remark that, independent of the field number and as far as only the integration is concerned, gates 2 and 4 have no active function. Hence, during integration, the basic concept of the device can be altered to the CCD illustrated in fig. 2 for respectively an odd field (a) and an even field (b) integration. Here the CCD gates are arranged into two groups, which are alternately used as blocking or integrating electrodes. Now the

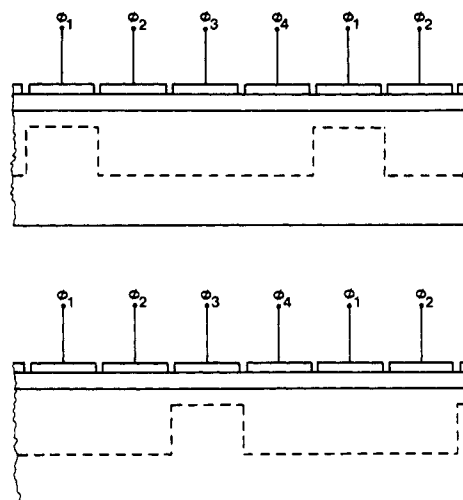


Figure 1.
Potential distribution during the charge integration of an odd field (a) and an even field (b) for a four-phase CCD-imager.

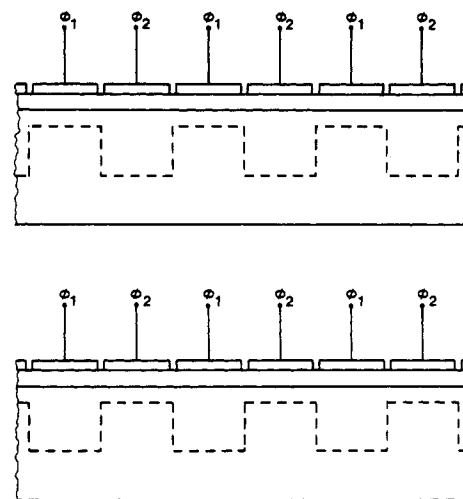


Figure 2.
Potential distribution during the charge integration of an odd field (a) and an even field (b) for the accordion CCD.

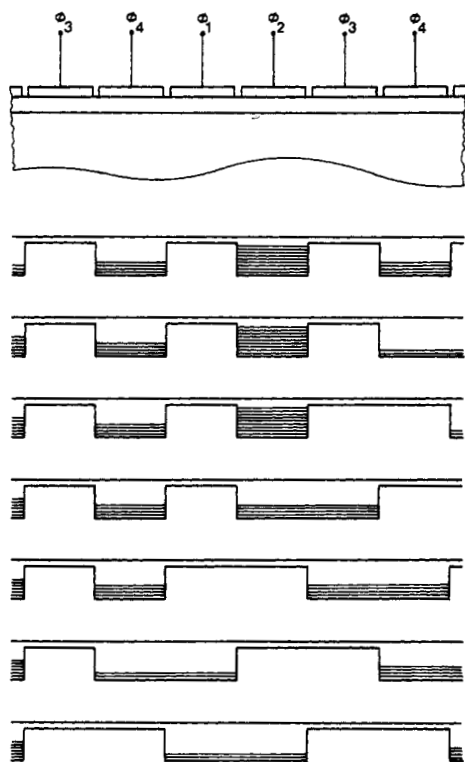


Figure 3.

The accordion read-out mechanism: starting from a two-phase integrating device and ending with a four-phase transporting system

status of all gates changes during the switching from one field to another.

The comparison between fig. 1 and fig. 2 demonstrates that the new device (further called the accordion CCD) has doubled the number of pixels without changing the area of the device. But problems arise when the new CCD has to transfer its collected charges. To avoid mixing of charge packets, a transport sequence reminding of the movements of an accordion is applied: the cells of the CCD are enlarged from two (a compact closed accordion) to four (a stretched accordion) electrodes per pixel, not for all the charge packets at once, but one after another, starting with the gates which are located nearest to the output. The accordion movement is illustrated in figure 3. This transport mechanism is maintained until all the charge packets are moving, or in other words, until the complete accordion is opened. All the cells in the system transform from a stationary two-phase integrating system (two electrodes per cell) to a transporting four-phase system (four electrodes per cell), one after another. When all charge packets are transported, the accordion has to be closed again before a next integration period can start.

A complete frame-transfer CCD contains two accordions: an image and a storage one, both synchronized. The transport from a "stretching image accordion" into a "closing storage accordion" is depicted in fig. 4. Only four lines of information are shown, which move from their places in the image section to their corresponding sites in the storage region.

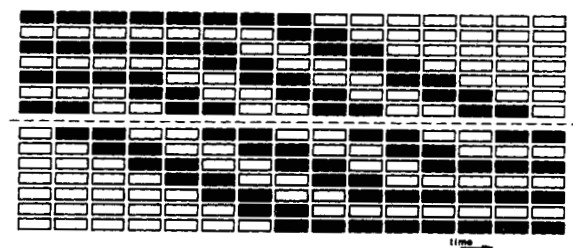


Figure 4.

Opening of the image accordion, run over into the storage accordion and closing of the latter.

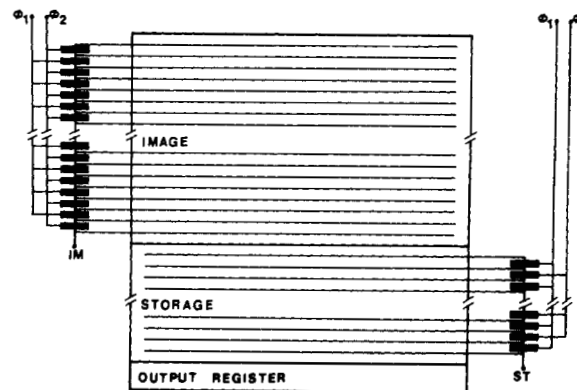


Figure 5.

Realization of the accordion drive-circuitry by means of digital shift registers which offers the right voltages to the CCD-electrodes.

REALIZATION OF THE ACCORDION

Driving of the accordion can be realized by applying the right voltages to the electrodes by means of two digital shift registers (fig. 5). These are built with a string of identical blocks. The inverting output of each block is connected to one electrode of the CCD and to the input of the next block. To force the data through the digital shift registers, only two clocks, ϕ_1 and ϕ_2 , common for the image and the storage section, are needed. IM and ST are used to enter the appropriate data, which result in an opening of the accordion and maintaining the four-phase transporting mode of the CCD. Keeping IM and ST constant is translated in a closing accordion and in an integration of the charges. Interlacing is achieved by the choice of the logic value of IM during the integration: IM = 0 and IM = 1 result respectively in a situation as depicted in fig. 2a and fig. 2b.

For an appropriate driving of all the individual electrodes of the accordion, the necessary peripheral electronics are integrated in CMOS-technology. The CMOS-CCD combination shown in fig. 6 affords the possibility to integrate the clocking circuitry on the CCD-chip without a too high on-chip heat dissipation.

The concept of one stage of the digital shift registers is shown in fig. 7. Three MOS-transistors are needed to drive one CCD-electrode: a CMOS-inverter with a MOS-switch. The output of the transistor combination is equal to the inverted input at the moment the clock goes active. Due to the gate capacitance,

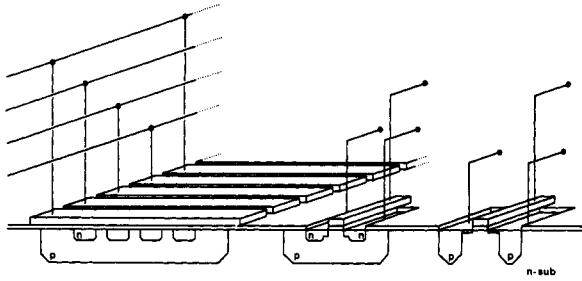


Figure 6.
The CMOS-CCD combination in one process.

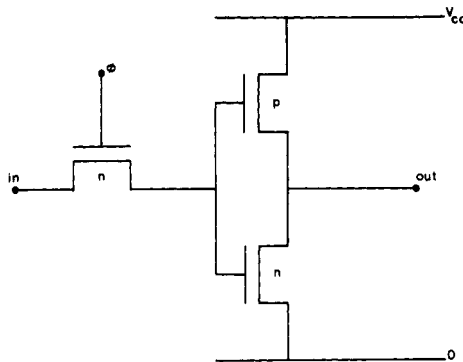


Figure 7.
The concept of one stage of the digital shift registers.

the output does not change for a sufficiently long time when the switch is closed or when the clock is inactive.

Because each CCD-gate has its own driver, a CMOS-inverter with its switch has to be placed in the vertical pitch of a CCD-gate. This is $5.5 \mu\text{m}$ in the imaging section and $4 \mu\text{m}$ in the storage region. These numbers are unreasonable and so four shift register cells are placed next to each other while the appropriate connections are passed to the CCD-frame. This arrangement can be seen on the micro-photograph in fig. 8: part of the driving periphery between the storage and the image section is shown.

DEVICE PERFORMANCES AND DEVICE FEATURES

The CCD is fabricated in a triple poly-Si n-buried channel process on a n-type substrate with an implanted p-well (1). A micro-photograph of the device is shown in fig. 9. The chip measures $5.46 \text{ mm (H)} \times 7.00 \text{ mm (V)} = 38.22 \text{ mm}^2$. The imager has $604 \text{ (H)} \times 588 \text{ (V)}$ interlaced pixels, each of $7 \mu\text{m (H)} \times 11 \mu\text{m (V)}$. These figures are achieved at $3.5 \mu\text{m}$ minimum dimensions. The same lay-out rules applied to a conventional CCD-imager, with the same number of pixels, result in a chip of 66.5 mm^2 .

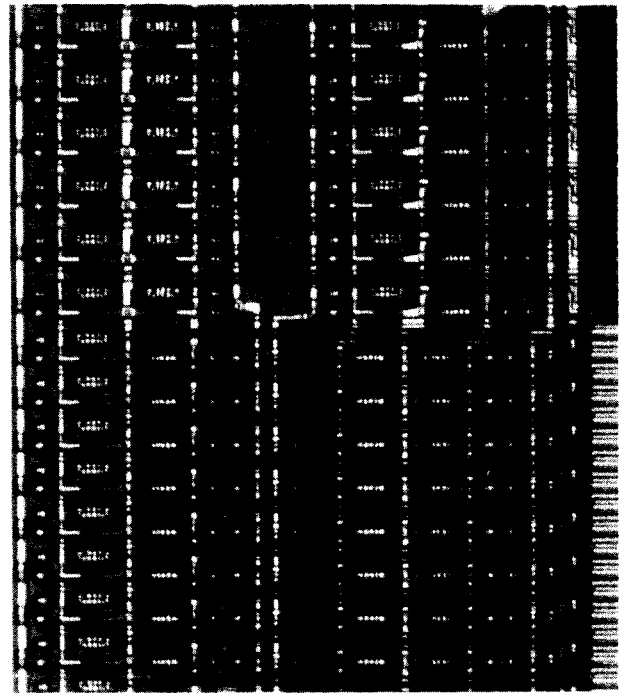


Figure 8.
Micro-photograph of part of the integrated driving periphery of the accordion CCD.

The performances of the device can be summarized as follows:

- 1) a low transport inefficiency (less than 5.0×10^{-5}),
- 2) a dark current of less than 1 nA/cm^2 at room temperature,
- 3) due to the extreme small image format, the present device has a relative low light sensitivity: 30 mV/lux sensor illumination (2800 K). But the accordion principle is of course applicable to other and bigger (e.g. $1/2''$ format) devices.
- 4) the on-chip amplifier has a response of $3.0 \mu\text{V/electron}$.

The unique features of this new accordion CCD are:

- 1) a very high pixel density although conservative lay-out rules are used. The minimum dimensions used on the accordion CCD-chip are $3.5 \mu\text{m}$ for poly-silicon strips and implantations, and $5 \mu\text{m}$ for metallization patterns.
- 2) compact and simple driving electronics: for all the vertical transports, less clocks are needed, with less constraints (the only requirement is that they are non-overlapping in time) and almost no capacitance to drive (a factor 100 lower).
- 3) define the frame travel time as the time needed to transport a complete frame from the image section to the storage section, and the line travel time as the time needed to transport a line from the image section to its corresponding location in the storage section. If the same transport frequency is used in comparison with a conventional four-phase device, the frame travel time is unchanged, but the line travel time is halved. This has the consequence that the smear halves.
- 4) the number of vertical transports is halved, because the number of gates is reduced with a factor of 2.
- 5) if a conventional frame-transfer CCD is redesigned into a corresponding accordion CCD with the same number of pixels on the same silicon area, then less poly-silicon elec-

trodes are needed to drive the image and the storage section. This is translated in a higher sensitivity, particularly for blue light.

6) for the same reason, the yield will be higher.

CONCLUSION

With a combined CCD-CMOS-technology and the aid of the accordion transport mechanism, we have developed a frame transfer CCD with ultra high density. 604 (H) x 588 (V) pixels are realized on 38.22 mm², although conventional lay-out rules are used.

ACKNOWLEDGMENT

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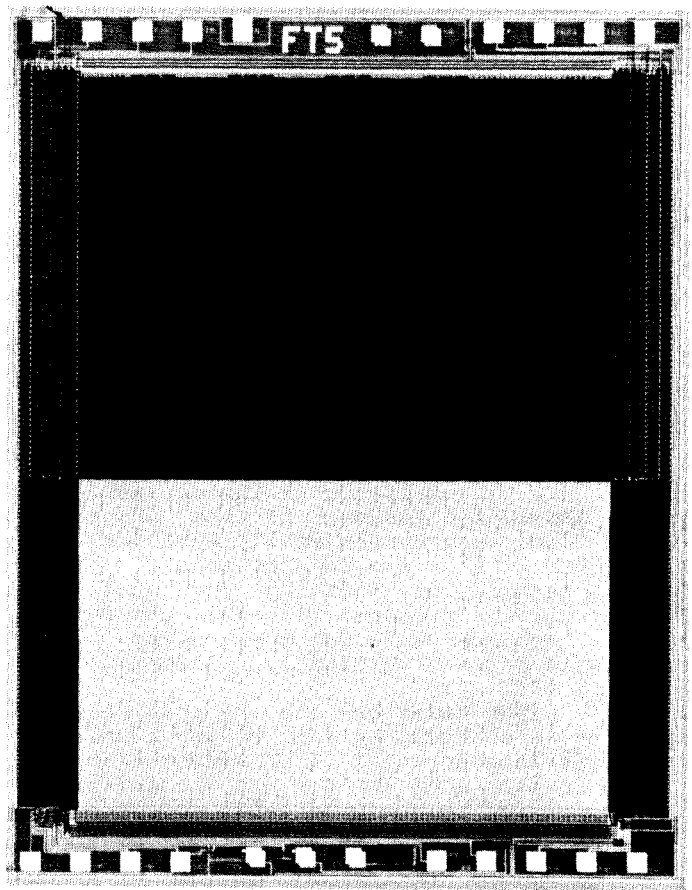


Figure 9.
Micro-photograph of the accordion CCD.

