The Tacking CCD: A New CCD Concept

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Abstract—**The Tacking CCD is a new type of charge transport mechanism that is suitable for junction- as well as MOS-type CCD's. A specific form, the Trenched Tacking CCD (TTCCD), promises high pixel density and high charge handling capability per unit of surface area. The TTCCD structure is suitable for making new types of solid-state image sensors with increased light sensitivity and there is the possibility of incorporating a vertical overflow drain. First samples of the TTCCD have been realized and its functionality has been confirmed.**

I. Introduction

Since the introduction of the bucket brigade device, many different concepts of charge-coupled devices have been developed. CCD's have found widespread application as delay lines, in electronic filters and oscilloscopes, and as optical sensors in facsimile apparatus and cameras. The CCD concepts most used today are the MOS types, as there are the surface CCD's and bulk CCD's [1]–[3], that can be further divided into the two-, three-, and four-phase CCD's, the meander CCD [4]–[7], the virtual-phase CCD [8], [9], and other types [10]–[12]. The charge handling capacity of all of these CCD's is limited to the oxide capacity times the effective surface area of the electrodes that are used for charge storage.

Even with the strong reduction in fixed pattern noise level and output amplifier noise level, image sensors still need a charge capacity of at least 50 000 electrons per pixel. To reach the standards set for high-definition television (HDTV) and electronic still picture, there is an urgent need to increase the amount of pixels on the light-sensitive surface area [13]. In these cases the charge storage capacity forms a serious obstacle to a further reduction in pixel dimensions. Moreover, at the same time light sensitivity and charge transport rates for HDTV image sensors have to increase. Hence there are a number of conflicting demands with regard to the design of CCD imagers, which cannot easily be met with the above mentioned CCD concepts.

Recently two new types of CCD's have been proposed [14], [15] that use trenches to increase the light sensitivity depth of the device and to increase the charge handling capability per unit of surface area. Both concepts have the disadvantage that the gates cross the trenches, thereby reducing the light sensitivity of the device.

In the initial phase of the development of CCD's it was suggested that the electrodes should be located on different sides of the charge transport channel [16]. In this paper we extend this to a new CCD concept that has the potential to reach the standards set for HDTV. As in the above mentioned publications, the charge handling capability is improved by using a trench to increase the charge storage area. However, with the new design concept it becomes possible to put the gates entirely into trenches, while simultaneously using the trenches as channel stops.

II. The Tacking CCD Mechanism

The new structure is characterized by two gates which are aligned parallel to the charge transport channel. The two gates are located on opposite sides of the charge transport channel. The potentials applied to these gates therefore create an electric field that is perpendicular to the direction of charge transport. Along each gate a dopant structure creates regions with a built-in electric field, with a charge storage, a charge transfer, and a charge blocking area. The neighboring storage areas are located on opposite sides of the charge transport channel. The new CCD structure is shown in Fig. 1.

For an n-channel CCD, the free charge carriers are collected in the charge storage area at the most positive gate. When the potential between the two gates is reversed, the free charge carriers are pushed towards the charge transfer area at the other side of the charge transport channel. From there the charge flows to the adjacent storage area. After another reversal of gate potentials, the free charge carriers will return to the first gate but, due to the built-in field, to the storage area of the next cell. The transport mechanism drives the free charge carriers through the bulk of the CCD. Since the charge storage is at some distance from the interface, the structure is a type of buried-channel CCD.

The transport path of the free charge carriers in this CCD closely resembles the movement of a sailing boat moving in an upwind direction. Therefore we named this type of charge coupled device a Tacking CCD.

Some different arrangements with the Tacking CCD concept are shown in Fig. 2. Fig. 2(a) shows a Trenched Tacking CCD (TTCCD), with the gates located in parallel trenches in a way that is of advantage for solid-state image sensors. By filling the trench with a refractory metal gate, it is possible to make a good channel-to-channel

Manuscript received September 6, 1990; revised January 28, 1991. The review of this paper was arranged by Associate Editor W. F. Kosonocky.

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IEEE Log Number 9143388.

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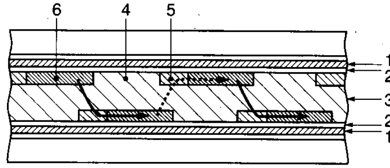


Fig. 1. Layout of the Tacking CCD. 1: gate, 2: insulation layer, 3: charge transport channel, 4: blocking area, 5: transfer area, 6: storage area. The arrows show the direction of charge transport by reversal of the gate potentials. Solid line: upper gate going negative, dashed line: lower gate going negative.

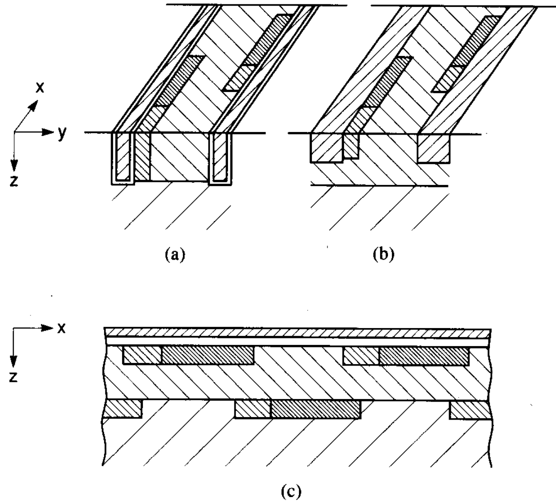


Fig. 2. (a) 3D layout of a Trenched Tacking CCD, the gates are positioned in trenches. The charge storage locations are found along the wall of the trench. (b) Junction Tacking CCD, the gates and its insulation layers are replaced by a p-n junction. (c) Tacking CCD with different types of gates in planar technology.

electrical as well as optical isolation. At the same time, due to low gate resistivity, a low RC time for the gates is achieved. Similar to a Junction CCD it is possible to replace the gates and isolation layers by a layer with dopant of the opposite sign. By replacing them on both sides, there is no need for an insulation layer. The charge transport channel itself constitutes the potential barrier between the gates. Fig. 2(b) shows this arrangement, with the two gates made by heavily doped p^+ areas parallel to the surface. Such a Junction Tacking CCD (JTCCD) can be made in GaAs and will be of advantage for radiation-hard devices, as for instance used for direct X-ray detection. Fig. 2(c) combines aspects of the TTCCD and JTCCD in a way that is most suitable for delay lines. Here the charge transport channel is turned 90° with respect to the previous examples. As is the case for all two-phase CCD's, the difference in potential between the first and second gate drives the charge transport. Therefore it suffices to apply a potential swing to the first gates, while holding the second gate at an intermediate potential. By clocking only the upper gate, the capacitance of a CCD line can be minimized.

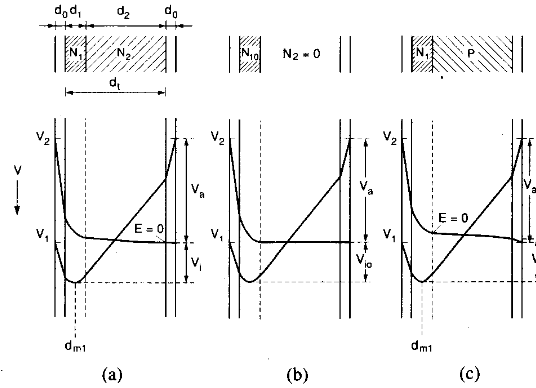


Fig. 3. Potential across the charge transport channel for homogeneously doped layers. (a) Upper part: dopant structure, d_0 insulation layer, d_1 charge storage area with dopant density N_1, d_2: remainder of charge transport channel, dopant density N_2, d_t: charge transport channel width. Lower part: Potentials, interval voltage swing maximized. $d_0 = 0.1$ μm, $\epsilon_r = 3$, $d_1 = 0.2$ μm, $d_2 = 0.8$ μm, $V_a = 5$ V, $N_2 = 5 \times 10^{14}$ cm^{-3}, $N_1 = 3.675 \times 10^{16}$ cm^{-3}, $d_{m1} = 0.0986$ μm, $V_i/V_a = 0.384$. Optimal dopant profiles have zero electric field at the interface with the insulation layer when the first gate is negative. (b) As in Fig. 3(a) for $N_2 = 0$. Lower part: $N_{10} = 4.125 \times 10^{16}$ cm^{-3}, $d_{m1} = 0.100$ μm, $V_{i0}/V_a = 0.4375$. (c) As in Fig. 3(a) with p-type substrate. Lower part: $P = 5 \times 10^{14}$ cm^{-3}, $N_1 = 3.775 \times 10^{16}$ cm^{-3}, $d_{mi1} = 0.0907$ μm, $V_i/V_a = 0.395$. With the first gate negative, the electric field is zero at the junction of storage area and substrate.

III. Dopant Profiles

To optimize the charge transport capacity of the Tacking CCD the externally applied potential swing on the gates has to be translated into a maximal internal voltage swing. This should be done in such a way that there exists no potential barrier when the free charge carriers have to cross from one side to the other.

A characteristic 1D cross section of the dopant structure for the TCCD is shown in Fig. 3. The charge transport channel has a total width d_t. As silicon is used as the substrate material, it has a dielectric constant of ϵ_{si}. The storage area, located along the first gate, has a depth d_1 perpendicular to the gate and is given a dopant concentration N_1. The remainder of the charge transport channel, of length $d_2 = d_t - d_1$, has dopant concentration N_2 (Fig. 3(a)) or P (Fig. 3(c)). The insulation layers between the substrate and the gates are assigned a thickness d_0 with dielectric constant $\epsilon_{ox} = \epsilon_{si}/\epsilon_r$.

If the potential on the first gate, at voltage $V1$, is positive with respect to the potential V_2 on the second gate, the potential reaches a maximum in the first layer at position d_{m1}. After the potentials on the gates are reversed the place of maximum potential shifts to the interface with the insulation layer at the other side of the charge transport channel. The voltage difference between the two positions is the internal potential swing V_i, that can be used for charge transfer and charge storage.

The ratio of the internal voltage swing V_i over the applied voltage $V_a = V1 - V2$ is maximized when $N_2 = 0$, as shown in Fig. 3(b). When the built-in voltages and work-function differences are neglected and homogeneously doped layers are used with $N_2 = 0$, the internal

voltage swing V_{i0} and optimal dopant concentration N_{10} are easily calculated. According to Fig. 3(b), we have

$$V_a = \frac{q}{\epsilon_{si}} N_{10}(\tfrac{1}{2}d_1^2 + \epsilon_r d_0 d_1) \tag{1}$$

with q the electron charge.

When the applied potentials are reversed, the internal potential reaches a maximum in the storage area and we have

$$V_a = \frac{q}{\epsilon_{si}} N_{10}(\tfrac{1}{2}d_1^2 + \epsilon_r d_0 d_1 - d_{m1}(d_1 + d_2 + 2\epsilon_r d_0) + d_1 d_2). \tag{2}$$

By solving N_{10} and d_{m1} out of (1) and (2) and noting that the internal voltage swing equals

$$V_{i0} = \frac{q}{\epsilon_{si}} N_{10}(\tfrac{1}{2}d_{m1}^2 + \epsilon_r d_0 d_{m1})$$

we find

$$V_{i0} = \frac{d_2(d_2 + 2\epsilon_r d_0)}{(d_1 + d_2 + 2\epsilon_r d_0)^2} V_a \tag{3}$$

with

$$N_{10} = \frac{\epsilon_{si}}{q} V_a / (\tfrac{1}{2}d_1^2 + \epsilon_r d_0 d_1)$$

as found from (1).

If the gates and insulation layers are replaced by a layer with dopant P_0, as was shown in Fig. 2(b) for a JTCCD, we can derive in a similar way the internal voltage swing V_{i0}

$$V_{i0} = \frac{d_2^2}{\left(d_1 + d_2 + \frac{N_{10}}{P_0} d_1\right)^2} V_a. \tag{4}$$

The equations for V_{i0} show that when the insulation layer thickness is small (or for the JTCCD: $P_0 >> N_{10}$), the conversion of the applied potential swing in an internal voltage depends mostly on the ratio of d_2/d_1.

Normally, storage and transfer areas will be constructed by the addition of dopant to these areas. Note that as long as an equal amount of additional dopant is added to both sides of the device, and d_2 is large with respect to d_1, the internal voltage swing remains about the same.

For a nonzero substrate dopant two different situations arise. When $N_2 > 0$, the optimal N_1 dopant concentration is reached when, with the first gate at V_2, the electric field is zero at the substrate to insulation layer interface as shown in Fig. 3(a). By neglecting build-in potentials and work-function differences, we find for this situation

$$V_a = \frac{q}{\epsilon_{si}} (N_1(\tfrac{1}{2}d_1^2 + \epsilon_r d_0 d_1) + N_2(\tfrac{1}{2}d_2^2 + (d_1 + \epsilon_r d_0)d_2)) \tag{5}$$

and when the potential is reversed we have, after rearranging the terms

$$V_a = \frac{q}{\epsilon_{si}} (N_1(\tfrac{1}{2}d_1^2 + (d_2 + \epsilon_r d_0)d_1) - N_1 d_{m1}(d_1 + d_2 + 2\epsilon_r d_0) + N_2(\tfrac{1}{2}d_2^2 + \epsilon_r d_0 d_2)). \tag{6}$$

From (5) and (6) we can find N_1 and d_{m1}. The internal potential swing is then found by

$$V_i = N_1(\tfrac{1}{2}d_{m1}^2 + \epsilon_r d_0 d_{m1}). \tag{7}$$

In Fig. 4(a), V_i is plotted for different values of N_2 as a function of d_t. The internal voltage swing V_i is less than V_{i0}, with the ratio of V_i/V_a decreasing when the background dopant is increased. The internal potential swing shows an optimum in the charge transport channel width for $N_2 > 0$, at which the ratio V_i/V_a is maximized. For $d_1 \downarrow 0$ the internal potential swing is

$$V_i = \frac{d_2 V_a}{d_2 + 2\epsilon_r d_0} - \frac{q}{2\epsilon_{si}} N_2 d_2^2. \tag{8}$$

The optimal width of the transport channel can then be approximated by

$$d_t \approx \sqrt[3]{\frac{2\epsilon_r \epsilon_{si} d_0 V_a}{qN_2}} - \frac{4}{3}\epsilon_r d_0. \tag{9}$$

For the different substrate concentrations the approximation of the optimum for $d_1 \downarrow 0$ is shown by the arrows at the bottom line of Fig. 4(a).

When the substrate dopant is of opposite sign to the dopant of the charge storage area, the situation changes, as is shown in Fig. 3(c). The optimum dopant concentration for the storage layer under this condition is reached when at the junction of the storage section with the p-type substrate the electric field vanishes. In this situation we have under similar conditions as for the previous one

$$V_a = \frac{q}{\epsilon_{si}} (N_1(\tfrac{1}{2}d_1^2 + \epsilon_r d_0 d_1) + P(\tfrac{1}{2}d_2^2 + \epsilon_r d_0 d_2)). \tag{10}$$

After the potential is reversed

$$V_a = \frac{q}{\epsilon_{si}} (N_1(\tfrac{1}{2}d_1^2 + (d_2 + \epsilon_r d_0)d_1) - N_1 d_{m1}(d_1 + d_2 + 2\epsilon_r d_0) - P(\tfrac{1}{2}d_2^2 + \epsilon_r d_0 d_2)). \tag{11}$$

After solving N_1 and d_{m1} out of (10) and (11), the internal potential swing is found by

$$V_i = \frac{q}{\epsilon_{si}} (N_1(\tfrac{1}{2}d_{m1}^2 + \epsilon_r d_0 d_{m1}) + P\epsilon_r d_0 d_2). \tag{12}$$

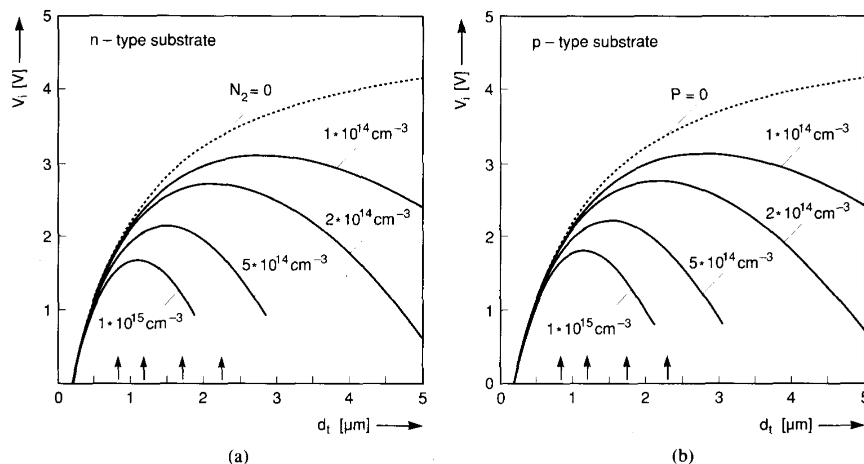


Fig. 4. V_i as function of background dopant density and charge transport channel width for $V_a = 5.0$ V, $d_0 = 0.1$ μm, $\epsilon_r = 3$, and $d_1 = 0.2$ μm (a) n-type substrate. Dashed curve: optimal $V_i(0)$ for $N_2 = 0$. Arrows show the approximation for the optimal transfer channel width by (9). (b) p-type substrate.

Fig. 4(b) shows that the reduction of the internal voltage swing for higher dopant of the substrate is nearly similar to the reduction as found for an n-type substrate. Only for the highest substrate dopant concentrations do slight differences arise. For $d_1 \downarrow 0$ the internal potential swing is given by a formula equivalent to (9) with P instead of N_2. So the optimum width of the transport channel is found to be independent of the sign of the substrate dopant.

In IC technology local implantations and subsequent diffusion steps are used to create the areas of preference. For the trenched tacking CCD the storage and transfer area can be realized by implanting the trench sideways, as shown in [17], [18]. In this way a more Gaussian type of dopant profile is realized. If the Gaussian dopant profile is given by

$$N(x) = N_0 \exp\left[-\frac{1}{2}\left(\frac{x}{\sigma_n}\right)^2\right]$$

where at the interface with the insulation layer $x = 0$, then the results as calculated for the homogeneous N_{10} layer can be translated, see for instance [20], [21].

By setting $d_2 = d_t - d_1$, $N_{10} = (\pi/4)N_0$, and $d_1 = \sqrt{(8/\pi)}\sigma_n$, we obtain from (1) and (3)

$$V_{i0} = \frac{\left(d_t - \sqrt{\frac{8}{\pi}}\,\sigma_n\right)\left(d_t - \sqrt{\frac{8}{\pi}}\,\sigma_n + 2\epsilon_r d_0\right)}{(d_t + 2\epsilon_r d_0)^2} V_a \quad (13)$$

with

$$N_0 = \frac{\epsilon_{si}}{q} V_a \bigg/ \left(\sigma_n^2 + \sqrt{\frac{\pi}{2}}\,\epsilon_r d_0 \sigma_n\right).$$

The result of this corresponds excellently with the results of computer simulations.

The diffusion depth of the implanted layers usually has the lower limit set by technological constraints to about 0.1 μm. Potential profiles with a large ratio of V_i/V_a are found for d_2 greater than about $2(d_1 + 2\epsilon_r d_0)$. When d_1 and d_0 are small, the width of the charge transport channel can be less then 1.0 μm.

The charge handling capability of the device is determined by the 2D area of the charge storage section as measured along the wall of the trench, and the part of the internal voltage swing that can be devoted to charge storage. If storage and transfer areas are defined by an implant of dopant, the depth of these areas is determined by the trench opening and the angle of implantation. This angle, to the normal of the implanted surface, may reach 70° [18] (see Section V). Therefore, the depth of the charge storage area, as measured along the wall of the trench, is limited by the present techology to about three times the width of the trench.

IV. 2D Simulations

The tacking CCD has a unit cell that consists of a charge blocking, transfer, and storage areas on opposite sides of the charge transport channel, with the cells staggered equidistantly along the device. The length of the three areas should be such that proper charge transport takes place. Moreover, holes should be removed from the charge transport channel to the substrate or to another specially constructed drain. Therefore, two- and three-dimensional simulations have been performed to check the feasibility of the TCCD concept.

As was noted in the previous section, the different areas of a TTCCD can be made by implantation and subsequent diffusion. The minimal value of σ_n and the width of the charge transport channel d_t were set by technological and lithographical constraints to $\sigma_n = 0.1$ μm and $d_t = 3$ μm, while d_0 was chosen to be 0.1 μm. Since the experimental device had a p-type background dopant of 5×10^{14} cm^{-3}, this background dope was used in the simulations. A

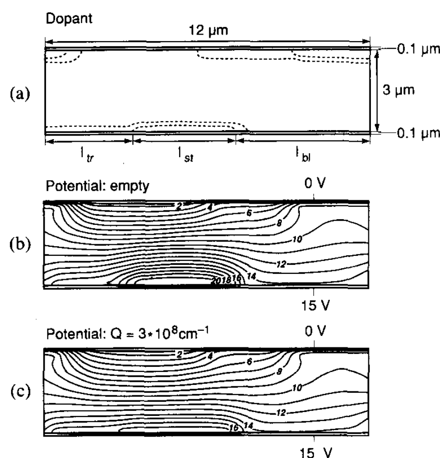


Fig. 5. 2D dopant structure and potential distribution for unit cell with Gaussian diffusion profiles. (a) Dopant structure: $d_{ox} = 0.1$ μm, $\epsilon_r = 3$, $d_t = 3.0$ μm, $N_{01} = 1.5 \times 10^{17}$ cm^{-3}, $N_{02} = 0.5 \times 10^{17}$ cm^{-3}, $\sigma_{01} = \sigma_{02} = 0.106$ μm, $N_2 = -5 \times 10^{14}$ cm^{-3}, $l_{st} = 4.0$ μm, $l_{tr} = 3.0$ μm, $l_{bl} = 5.0$ μm, $l_t = 3.0$ μm. (b) Potential distribution, $V_a = 15$ V. The potential distribution is periodic, no free charge. (c) Potential distribution with free charge density in storage area of 3×10^8 per centimeter of trench depth.

p-type background was chosen in order to drain the holes to the bulk, however the relatively high concentration complicated the transport. Therefore, special attention was paid to the determination of the lengths and the amount of additional implant for the three different areas.

The total cell length was 12 μm, with the length of the charge storage area of 4 μm, the length of the charge transfer area of 3 μm, and a charge blocking area of 5 μm.

Fig. 5(a) shows the 2D layout of the unit cell. The transfer and blocking areas prohibit backwards charge transport when the potential on the gates is reversed. The lengths were chosen to give a sufficient charge storage capability for the storage area. Lithographical details were limited to 3 μm, except for the width of the trench, which was defined by electron-beam pattern generation. Based on simulations, an overlap between the charge storage area and the charge transfer area on the other side of the charge transport channel of 0.5 to 1.0 μm was found optimal. The transfer and storage areas were n-type doped with an effective implantation dose of about 1×10^{12} and 2×10^{12} cm^{-2}. Results of the simulations with $V_a = 15$ V are shown in Fig. 5(b) and (c). Fig. 5(b) shows the potential distribution when there are no free charge carriers. Good potential characteristics were easily found, however the p-substrate dopant did reduce the effective internal voltage swing.

When electrons are stored in the storage area, as shown in Fig. 5(c), the potential distribution in the charge transfer area is relatively unchanged. For this simulation a charge content of about 3×10^8 electrons per centimeter of trench depth was found, giving over 100 000 electrons charge handling capability for an effective trench depth of more then 4 μm. Note that the TCCD is a bulk-CCD concept. Free charge is stored in the storage section some distance from the interface with the isolation layer. The charge transport is limited to the volume between the trenches, away from the upper surface, by implanting a shallow p-dopant at the upper surface.

V. Design and Technology

A single-line TTCCD is designed with input and output sections as shown in Fig. 6. The TTCCD line has a total length of 128 unit cells. Contacts to the TTCCD are: *IN:* input source, *IG:* input gate, *FI*1: first trench, *FI*2: second trench, *RG:* reset gate, *LS:* light shield, *RD:* reset drain, V_{DD}: positive power supply to the output circuit, and the *SN* leakage current drain, P_{sub}: negative power supply to output circuit and substrate, *OUT:* output, V_{CC}: negative power supply to the current source of the output source-follower.

An enlargement of the input section is shown in Fig. 7(a). The input gate connects the input source to the first storage area, located along the lower trench. The input can be blocked by lowering the potential on the input gate.

Connection to the trench gates is made by small additional trenches as shown in Fig. 7(b). The slab of poly-Si extending out of the trench is contacted by a second poly that connected to an Al layer. Only gate *FI*1, located in the upper trench, is clocked. *FI*2 is fixed at an intermediate voltage. The signal input is accomplished by clocking the input gate synchronously with the first trench gate and applying a potential pulse of various durations to the input source itself.

The last storage section at the *FI*2 gate is in direct contact with the floating diffusion. As this gate is not clocked, the charge packet is injected onto the floating diffusion when the clocked phase goes negative. The floating diffusion is coupled to the first gate of a conventional output circuit, as was described elsewhere [22]. The floating diffusion is reset to the reset drain potential by means of a reset gate.

The input and output circuitry is defined by conventional IC technology. Lithography to define the trenches is performed on an electron-beam pattern generator. The trenches were aligned parallel to the 110-wafer flat. This way a vertical trench etched into the wafer exposes an 100-trench wall along the active region of the TTCCD. The trenches are formed by reactive ion etching with an oxide mask of about 0.5 μm. A closeup of the trenches that defined the charge transport channel is shown in Fig. 8. The trenches have a width of 1.0 μm and a depth of about 4.0 μm. To define the implantation for the storage and transfer areas a method as described by Peek [19] was followed. First the trenches are filled to the surface with a photoresist. There upon the trenches are covered with a masking layer of Al as shown in Fig. 9(a). After defining the openings in the mask for the transfer and storage areas, the filler is removed from the trench, as shown in Fig. 9(b). The uncovered sidewall of the trench is implanted

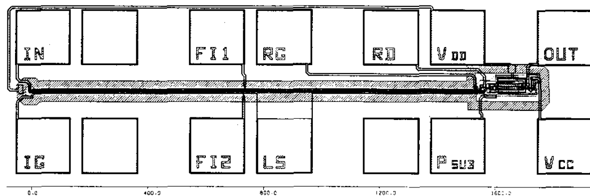
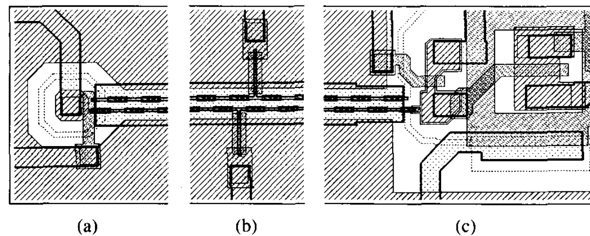


Fig. 6. Mask layout of single-line Trenched Tacking CCD with output circuit. 128 cells, unit cell length of 12 μm, charge transport channel width of 3 μm, and trench width of 1 μm.



(a) (b) (c)

Fig. 7. Closeup of layout for input structure, trench contacts, and output structure. (a) Input. (b) Trench contacts. (c) Output structure.

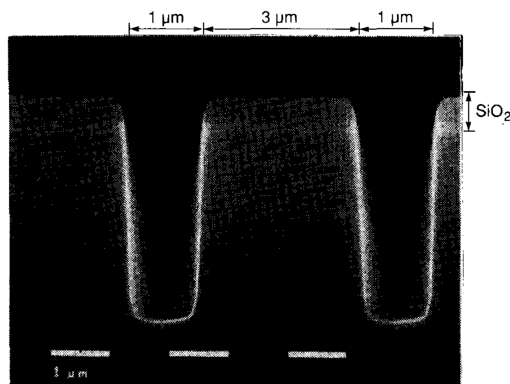
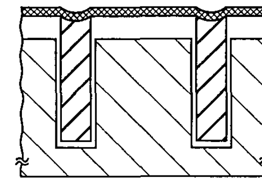
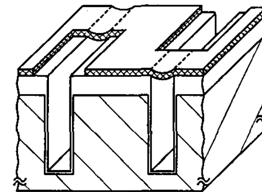


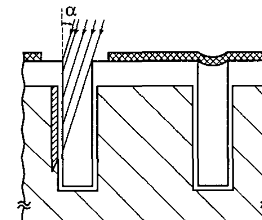
Fig. 8. Cross section of trenches and charge transfer channel. The oxide mask of 0.5 μm is visible on the silicon surface.



(a)



(b)



(c)

Fig. 9. Local implantation of trenches [19]. (a) Trench filled with photoresist and covered by Al. (b) After etching of Al and removing photoresist. (c) Local implantation of trenches, $\alpha = 17.5°$.

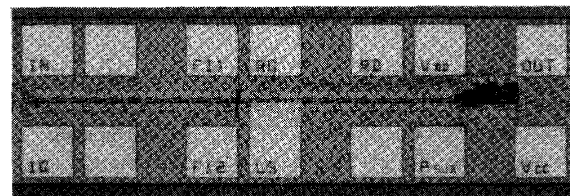


Fig. 10. Photograph of the single line Trenched Tacking CCD.

through the mask openings at an angle of 17.5° with the wall of the trench shown in Fig. 9(c). The implantation of the arsenic dose of 6×10^{12} cm^{-2} is obtained from a High Energy Implanter at 300 keV through 10-nm SiO_2. The procedure is repeated for an additional implant to the storage areas.

Afterwards an insulation layer of 0.1-μm SiO_2 is grown on the inside of the trenches and the trenches are filled with the poly-Si that defines the gates *FI*1 and *FI*2. The active region is covered by an insulation layer and an Al light shield. The light shield could be used to suppress spurious transfer along the upper surface of the charge transfer channel by setting it at an negative voltage. Fig. 10 shows a photograph of the device as used in our experiments.

VI. Measurement Results

The output of the TTCCD was coupled to an output follower circuit and measured on an oscilloscope. The output consists of the signal of the charge packet on the floating diffusion, superposed on the crosstalk of the potential swing applied to the gate in the first trench and the crosstalk of the reset gate. The bandwidth of the output structure, measured by opening the reset gate and applying a test signal to the reset drain, exceeded 10 MHz. The sensitivity of the output was about 4 μV/electron. Synchronously with the clocking of the TTCCD gate, the reset gate was clocked with a 10-V potential swing. Crosstalk of the reset gate with this clocking voltage was in the order of 150 mV. Output waveforms for a 20-V, 10-μs clock, applied to one of the trench gates only, are shown in Fig. 11. The crosstalk of the potential swing of −5 V

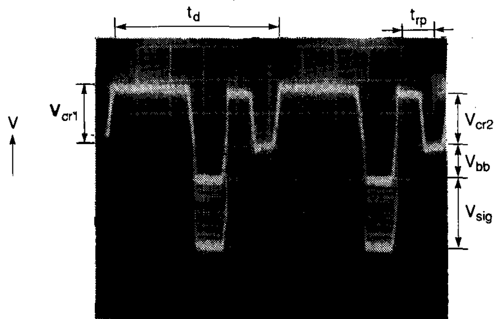
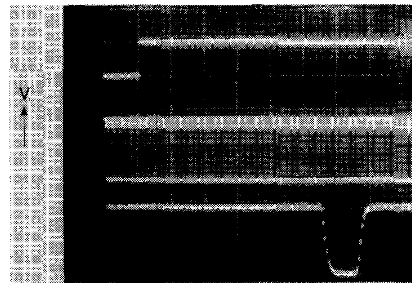


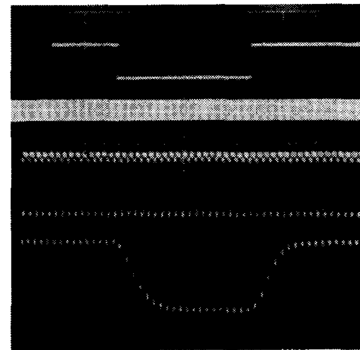
Fig. 11. Oscilloscope trace of output signal (*H*: 0.2 μs/div, *V*: 50 mV/div). Clocking period t_{cl} = 10 μs, reset gate pulsewidth t_{rp} = 0.2 μs. V_{cr1}: crosstalk of trench gate, V_{cr2}: crosstalk reset gate, V_{bb} bias-charge voltage, V_{sig}: output signal voltage.

to +15 V was about 100 mV. The second trench gate was set at 5 V and the reset drain at 16 V. Charge handling capability was found limited to about 40 000 electrons for a clocking voltage of −5 V to +15 V and could not further be increased with higher clocking voltages.

Up to a clocking frequency of 1 MHz, the various stages in the output are clearly separable on the oscilloscope. Fig. 12(a) shows the output of the TTCCD after 256 transfers (128 cells) that resulted from a square-wave input signal of 20 clocking periods at a clocking rate of 100 kHz. A relatively large transport inefficiency was noted. An enlargement of the input and the delayed signal is shown in Fig. 12(b). Input was performed by clocking the input gate synchronously with the trench gate, and applying a pulse to the input. A bias charge of about 10 000 electrons was added to the signal to improve the charge transport efficiency. The delayed pulse has a frequency response [23] that corresponds with a transport efficiency of about 0.990 per stage. Up to 1 MHz the transport efficiency was relatively independent of the clocking period. Increasing the voltage swing did not reduce the transport inefficiency further.



(a)



(b)

Fig. 12. (a) Input and output signal (*H*: 200 μs/div) for t_{cl} = 10 μs. Total delay time equals 1.28 ms. (Input: *V*: 0.1 V/div, output: *V*: 50 mV/div.) (b) Enlargement of input and output waveform (*H*: 40 μs/div).

VII. Discussion

A straight slope of the trench, square to the surface of the wafer, would have exposed the 100 surface. The trench wall was found slightly tapered (Fig. 8), this indicates a large number of surface defects. As indicated by the 1D calculations of characteristics of dopant profiles, a charge transport channel width of 3.0 μm is not optimal for a TTCCD with an background dopant of 5×10^{14} cm^{-3}. Therefore, a considerable increase in charge handling is expected from a lower doped substrate with optimal dopant concentations. Measurements of the process control module showed that in the first devices an insufficient amount of dopant has reached the storage and transfer areas, as was also indicated by the limited charge handling capability. A considerable amount of dopant was found at the bottom of the trench. This will have created additional pockets through which the charge packet could leak. Moreover too low a dose, by decreasing the potential differences between the blocking, transfer, and storage areas, facilitates backwards electron flow and limits the charge handling capability.

An increase of charge handling capability is possible by a further reduction in the thickness of the insulation layer along the wall of the trench and an optimizing of the dopant profiles. As lithography has quickly grown in the past decade, it has become clear that the width of the trench and charge transport channel can be reduced further. For a background dopant of 5×10^{14} cm^{-3} a charge transport channel width of 1.5 μm is optimal.

Modern solid-state imagers require a vertical overflow drain to eliminate charge from overexposed cells. As shown in Fig. 13 this can be realized by using a second gate that controlls an overflow drain at the bottom of the trench. These measures would also prevent charge from leaking along the bottom of the trench. More research is needed to overcome the technological difficulties associated with such a device.

VIII. Conclusions

The Tacking CCD is a new CCD concept that promises high charge handling capability, high cell density, and high light sensitivity. Preliminary results with a 128-cell

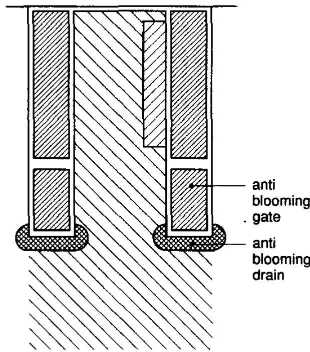


Fig. 13. Trenched Tacking CCD structure with second gate for vertical antiblooming mechanism.

delay line have proven the feasibility of the Trenched Tacking CCD concept. A charge handling capability of 40 000 electrons was found with charge transport efficiency of 0.990 per stage and a bias charge of 10 000 electrons. By selecting a p-type substrate of lower background concentration, the charge handling capability of our devices can be considerably increased. The measured transport inefficiency was attributed to a doping density too low for transfer and storge sections and an unexpectedly large amount of dopant found at the bottom of the trenches. Experiments therefore are starting to optimize the doping of the trenches and to straighten the vertical walls of the trench.

Acknowledgment

The authors would like to thank J. Politiek, M. G. Collet, and the Philips Research Laboratories for the facilities to carry out the experiments.

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