A 35-mm Format 11 M Pixel Full-Frame CCD for Professional Digital Still Imaging

Jan T. Bosiers, *Senior Member, IEEE,* Bart G. M. Dillen, Cees Draijer, Agnes C. Kleimann, Frank J. Polderdijk, Marc A. R. C. de Wolf, Wilco Klaassens, Albert J. P. Theuwissen, *Fellow, IEEE,* Herman L. Peek, *Member, IEEE,* and Hein Otto Folkerts

***Abstract*—To meet the demand for higher resolution in professional digital imaging, an 11 M pixel, 35-mm format full-frame CCD image sensor was developed as an upgrade for an existing 6 M pixel CCD. This paper presents the device requirements, the architecture, modes of operation, and extensive evaluation results.**

***Index Terms*—Charge coupled devices, color, digital still, image sampling, image sensors, sensitivity.**

I. Introduction

In 1994, a 35-mm film compatible 6 M pixel full-frame CCD was developed, originally intended for use in professional digital camera backs, and now also being used in high-end prosumer digital camera applications [1], [2]. This imager has 3072 (H) $\times$ 2048 (V) active pixels of 12 μm $\times$ 12 μm, resulting in an image area of 36×24 mm^2, corresponding to the 35-mm standard film format. In response to the demand for higher resolution, a new 11 M pixel imager, having 4008 (H) $\times$ 2672 (V) pixels of 9 μm $\times$ 9 μm in the same 36×24 mm^2 imaging format was developed. In addition to the optical and electronic system compatibility with the existing 6 M pixels sensor, the option of reading out vertically subsampled images was added in the new design.

II. Requirements For Professional Digital Still Imaging

For professional digital still imaging, compatibility with existing lens systems is mandatory. For 35-mm SLR cameras, this requires large image sensors with an active image area of 36 mm $\times$ 24 mm, leading to chip sizes of almost 1000 mm^2. This implies the use of a CCD technology to fabricate these devices that can combine high production yields with excellent imaging properties. To achieve competitive imaging quality, a high pixel count must be combined with good sensitivity, low dark current, high linear dynamic range ($\geq$72 dB, i.e., $\geq$12 bits), good overall linearity (less than 1% deviation up to saturation from "photons in" to "mV out"), excellent overexposure control ($\geq$1000 $\times$ overexposure), and instant electronic shutter (for high image capture rate and flexible readout modes). The compatibility with existing SLR camera lenses also implies an excellent angular response for incident light with chief ray angles up to 30°. For good color reproduction, an RGB Bayer color pattern is applied. The application also requires flexibility in operation, such as very fast full-resolution readout or subsampled readout.

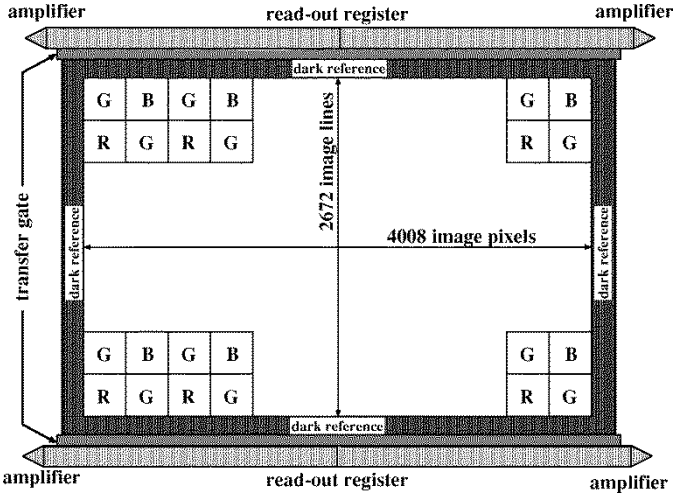

Fig. 1. Basic concept of a 11 M 35-mm full-frame CCD imager for professional digital imaging.

III. CCD Concept, Design, and Operation

A. Sensor Architecture

Fig. 1 shows the basic architecture of the 11 M pixel full-frame imager. Similar to the 6 M pixel CCD concept presented earlier [1], it contains a four-phase image section, two three-phase read-out registers and four output amplifiers. In addition, the new imager now has a transfer gate between the image section and the readout registers. This significantly increases the operational flexibility, as will be shown. Since the size of the imager exceeds the field of view of the lithographic equipment, stitching was required to obtain this format [1], [3]. Table I summarizes the device design specifications.

B. CCD Technology

A CCD technology using three layers of polysilicon and one metal layer is used to fabricate these sensors [4]. A second layer

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J. T. Bosiers, B. G. M. Dillen, C. Draijer, A. C. Kleimann, F. J. Polderdijk, M. A. R. C. de Wolf, W. Klaassens, and H. L. Peek are with DALSA B.V., 5656 AA Eindhoven, The Netherlands (e-mail: jan.bosiers@ dalsa.com).

H. O. Folkerts is with Philips Semiconductors, Eindhoven, The Netherlands.

A. J. P. Theuwissen is with the Philips Semiconductors, 5656 AA Eindhoven, The Netherlands and also with Delft University of Technology, Delft, The Netherlands.

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TABLE I
OVERVIEW OF CCD DESIGN CHARACTERISTICS

Number of active pixels	4008 (H) × 2672 (V)
Pixel Size	9.0 × 9.0 μm^2
Optical Size	36.072 mm (H) × 24.048 mm (V)
Technology	3 layers of polysilicon, one (+one) metal
Minimum feature size	0.5 μm
Color filters	RGB Bayer
Output Amplifiers	three-stage source followers (4×)
Voltage Adjustments	1 (substrate voltage)
Number of image phases	4 (split top and bottom)
Number of output register phases	3 (split left and right)
Full-resolution readout modes	Single output
	Single mirrored output (V and/or H)
	Dual output top-bottom
	Dual output left-right
	Four-quadrant output
Vertically sub-sampled readout reduction factor	RGB out, binned or non-binned selectable by pulse pattern

of metal is used only for optical pixel separation, see below. The aperture ratio is 80%. The buried n-channel CCD is made in a diffused p-well on an n-type substrate. Minimum feature size is 0.5 μm. A Bayer R-G-B color filter pattern is applied.

Note that a four-phase, two-poly pixel cell design is advantageous over a three-phase, three-poly design with respect to maximum charge capacity (always at least two gates, i.e., 50% of the pixel area, are used for charge storage), aperture ratio and sensitivity during integration (three out of four gates integrating), and symmetry of angular response.

C. Image Pixel Design

Fig. 2 shows a top view and a cross section of the image pixel. The pixel size is 9.0×9.0 μm^2, and a four-phase electrode structure is adopted $(A1 \ldots A4)$, using two layers of polysilicon. During integration, three gates are set integrating (high voltage), and one gate is blocking (low voltage). The optical pixel separation is enhanced by a thin layer of metal just under the color filters.

The vertical npn-structure ensures good highlight handling: blooming is prevented by using the n-substrate as a vertical overflow drain (VOD) [5]. Fig. 3 shows the potential profile versus depth in silicon under an integrating gate at full well capacity, under an integrating gate with an empty well, and under a blocking gate. The fourth curve shows the potential distribution at "charge reset" (electronic shutter) conditions. Electronic shuttering is performed to define the start of the exposure time: a positive pulse on the n-substrate (VNS) while all four image gates are at the low level drains all electrons previously collected in the image pixels to the n-substrate.

D. Readout Register and Output Amplifiers

The two read-out registers are designed as three-phase CCD registers using three layers of polysilicon. The four identical output amplifiers are conventional three-stage source followers. The capacitance of the floating diffusion detection node was designed to achieve a conversion factor at the output node of 12 μV/electron. This results in 1200 mV out at linear saturation level, matching the requirements of the off-chip signal processing ICs.

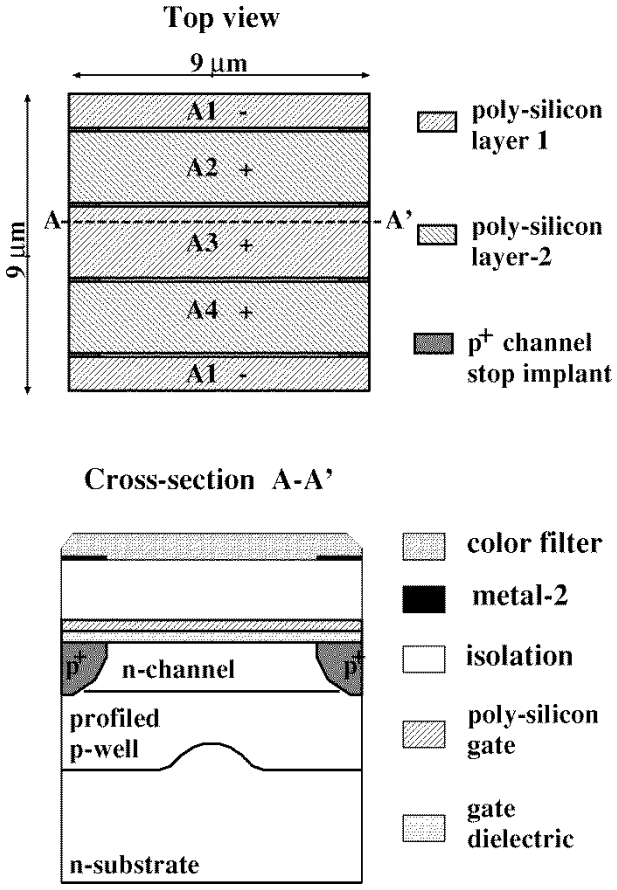

Fig. 2. Top view and cross-section of CCD pixel.

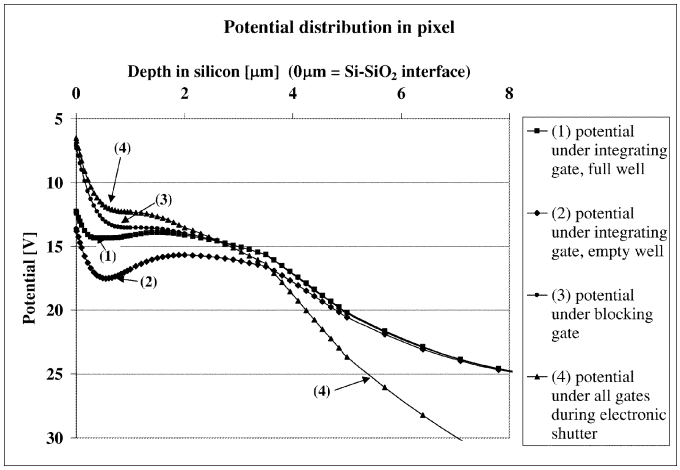

Fig. 3. Potential distribution in pixel.

E. Sensor Modes of Operation

Basic Mode of Operation: In the simplest mode of operation, a full-resolution, single-shot image with 11 M pixels resolution is obtained by first exposing the CCD to the scene through the

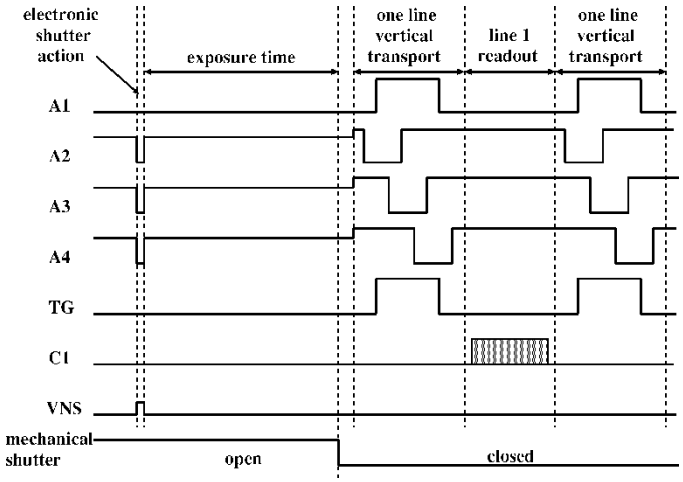

Fig. 4. Clock pulses for full-resolution readout.

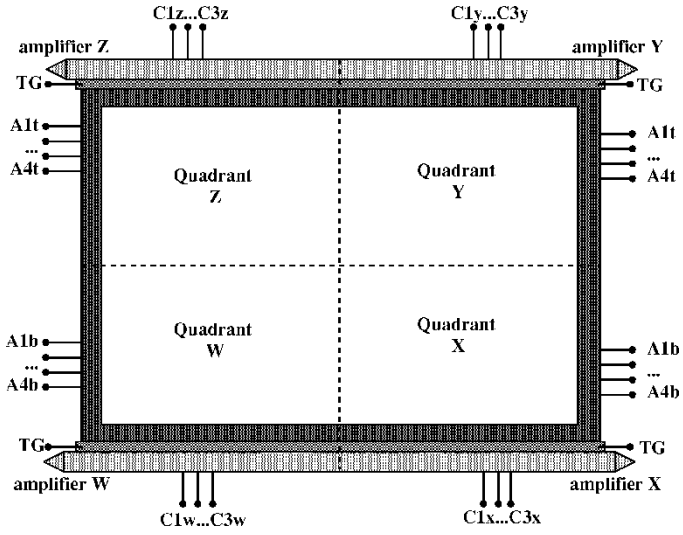

Fig. 5. Image and readout register connections.

camera lens, then closing the camera mechanical shutter, and finally reading out the image, using only one of the read-out registers and one of the corresponding output amplifiers. Fig. 4 shows the required clock waveforms. Using one output amplifier, a frame rate of about two images/s can be achieved at 25 MHz pixel frequency.

High-Speed Readout at Full Resolution: As shown in Fig. 5, the image section has two sets of clock connections ($A1t \ldots A4t$ for the top half, $A1b \ldots A4b$ for the bottom half). A split in the clock connections located at the horizontal center of the image area allows a left-right split readout: for each of the two readout registers: horizontal clock connections ($C1w \ldots C3w$ for bottom left, to $C1z \ldots C3z$ for top left). Default readout is obtained through the bottom-left amplifier (amplifier W) by applying four-phase transport clock signals $A1, A2, A3$ and $A4$ to the image electrodes as $A1 = A1t = A1b$, $A2 = A2t = A2b$, etc, and three-phase readout clocks signals $C1, C2$, and $C3$ to electrodes as $C1 = C1w = C1x$, $C2 = C2w = C2x$, etc. For this readout mode, the top readout electrodes (suffix "y" and "z") need not be connected.

TABLE II
OVERVIEW OF CLOCK CONNECTIONS FOR DIFFERENT READOUT MODES

	bottom left	top left	bottom left & bottom right	top right
	Amp W	Amp Z	Amp W& Amp X	Amp Y
A1b	A1	A1	A1	A1
A2b	A2	A4	A2	A4
A3b	A3	A3	A3	A3
A4b	A4	A2	A4	A2
A1t	A1	A1	A1	A1
A2t	A2	A4	A2	A4
A3t	A3	A3	A3	A3
A4t	A4	A2	A4	A2
C1w	C1	–	C1	–
C2w	C2	–	C2	–
C3w	C3	–	C3	–
C1x	C1	–	C2	–
C2x	C2	–	C1	–
C3x	C3	–	C3	–
C1y	–	C1	–	C2
C2y	–	C2	–	C1
C3y	–	C3	–	C3
C1z	–	C1	–	C2
C2z	–	C2	–	C1
C3z	–	C3	–	C3

Single readout to any of the other three amplifiers (X, Y, Z) is achieved by changing the appropriate transport directions. To reverse the transport direction in the four-phase image pixels, phases $A2$ and $A4$ need to be interchanged. Interchanging phases $C1$ and $C2$ will change the transport direction in the three-phase readout registers.

To decrease the readout time, the four quadrants of the image area can be read out through the four separate outputs, allowing an almost four times faster readout. Only a "left-right" or "top-bottom" split-readout using two separate outputs is also possible. Table II shows some examples of readout with corresponding clock connections.

Readout at Reduced Vertical Resolution: As will be illustrated, the introduction of a transfer gate allows the generation of subsampled images, both nonbinned or binned, while maintaining the RGB Bayer pattern. In normal operation, the transfer gate (TG) is synchronised with the image clocks, e.g., for readout through the bottom register the clock pulse $A1$ is applied to electrodes $A1b$, $A1t$ and TG. However, when the transfer gate is switched off during one cycle of the vertical transport, charge from a selected image line can be dumped to the substrate. Fig. 6(a) shows a schematic top view of one column of the imager at the image-to-serial transition, for a subsampling sequence without charge binning that reduces the vertical resolution by a factor of three. At $t1$, a first charge packet $Q1$ has been transported into the readout register ($A1$ pulse applied to TG), and is read out. If now TG is switched off during the next cycle of the vertical transport $(t2)$, $Q2$ will first be confined under the last $A4$ electrode only, and finally be drained

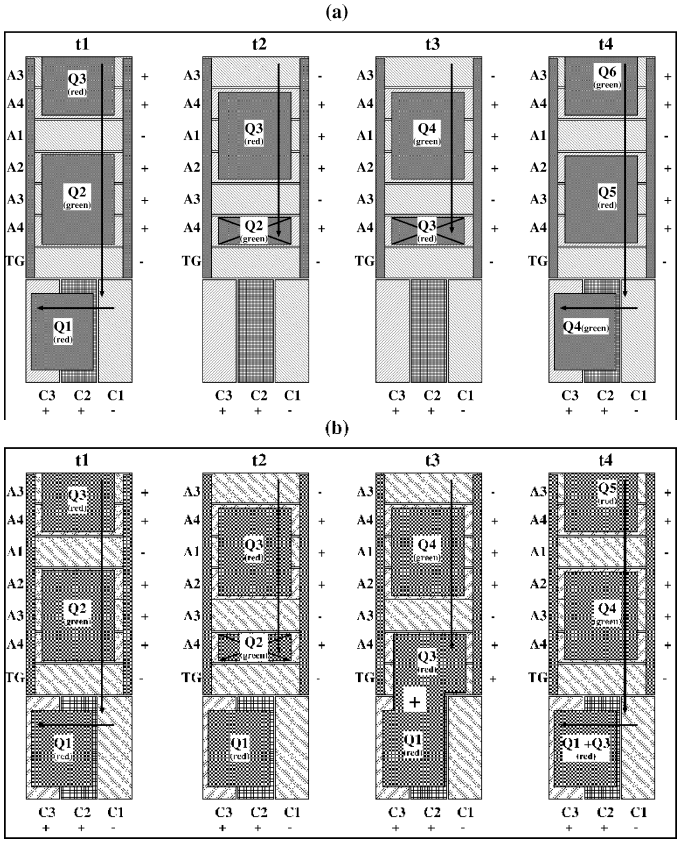

Fig. 6. Schematic representation of vertical subsampling (a) without and (b) with binning.

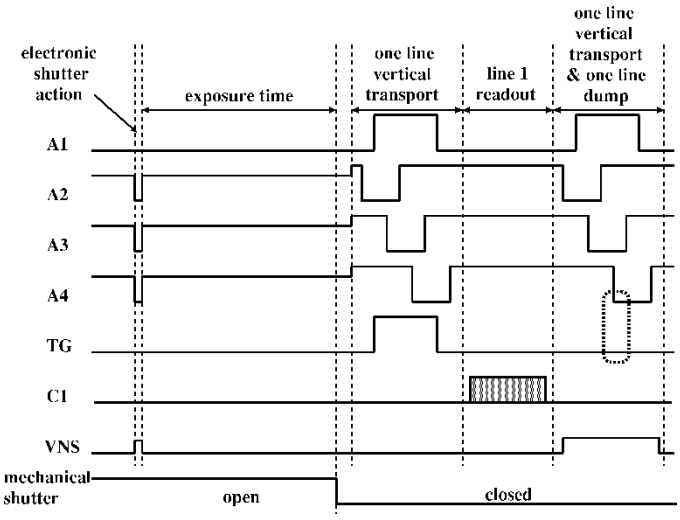

Fig. 7. Clock pulses for vertically subsampled readout without binning.

to the substrate when the $A4$ pulse is switched off. At $t3$, the same happens with packet $Q3$. Next, charge packet $Q4$ is transported into the readout register, and read out. The corresponding waveforms for one readout and one dump cycle are illustrated in Fig. 7. By reading out one line and dumping the contents of the next two lines (i.e., 1 : 3 vertical subsampling), the RGB pattern is maintained. Fig. 6(b) shows a similar sequence, but with charge binning. The charge from line 1 is read into the readout register $(t1)$, then the charge of line 2 is dumped $(t2)$. Next the charge of line 3 is added to line 1 $(t3)$. At $t4$, the sum is read out. Again, an image with one-third vertical resolution is generated, and the RGB color pattern is maintained. In the next cycle, lines four and six are binned, and line five is dumped. A higher ratio of subsampling, both with or without binning, (e.g 1 : 11, to achieve an image of 242 lines), can be simply achieved by modifying the pulse patterns. The principle of operation is identical to the vertical subsampling at the image-storage transition presented in [6].

These subsampled images can be used as electronic "viewfinder" (in combination with a mechanical shutter if a smearless image is required), and for focus and exposure control at higher frame rates. Subsampling with binning can also be used to enhance the S/N ratio of images at low light conditions. During the combined frame shift and subsampling, the "electronic shutter pulse" is applied to the n-substrate, as it is required to dump the charge packets to the substrate at the image to register transition. Because of this pulse, the maximum charge capacity in monitor mode is about 25% to 40% smaller than in full resolution mode: the overflow barrier (Fig. 3) for charge packets that are not dumped is reduced. However, the dynamic range of 65 dB still exceeds by far the requirements for this mode of operation.

It should be noted that subsampling without binning can be easily achieved in CMOS APS sensors. Subsampling with binning in the charge domain is much more difficult to achieve. One solution requiring extensive design changes, and still allowing only pre-designed binning factors, and not suitable for RGB patterns, has been presented in [7].

Auto-Focus Mode: The combination of vertical subsampling and instant electronic shutter offers the possibility to operate the sensor in "auto-focus mode." With the correct pulse patterns, selected blocks of lines of the sensor can be read out to obtain scene information that can be used for the camera auto-focus system. Two examples are shown in Fig. 8. In Fig. 8(a), the center 200 lines only of the imager are read out. The lines below the selected area are dumped by subsampling before the selected lines are read out, the lines above are dumped by electronic shutter as soon as the last selected lines have been read out. At 50 kHz vertical frequency and 25 MHz pixel clock, this allows the generation of 15 "auto-focus images" per second using a single output. Fig. 8(b) shows an example allowing auto-focus control on five areas of the scene (center and four corners).

IV. Evaluation Results

In this section, extensive evaluation results of the 11 M pixel CCD imager will be presented. All aspects of sensor performance relevant to the use in a digital imaging system will be reviewed.

A. Operating Conditions

Table III shows the typical operating conditions for this sensor.

B. Image Pixel Evaluation

Charge Capacity: The charge capacity of CCDs for professional applications is a very important competitive issue, as it

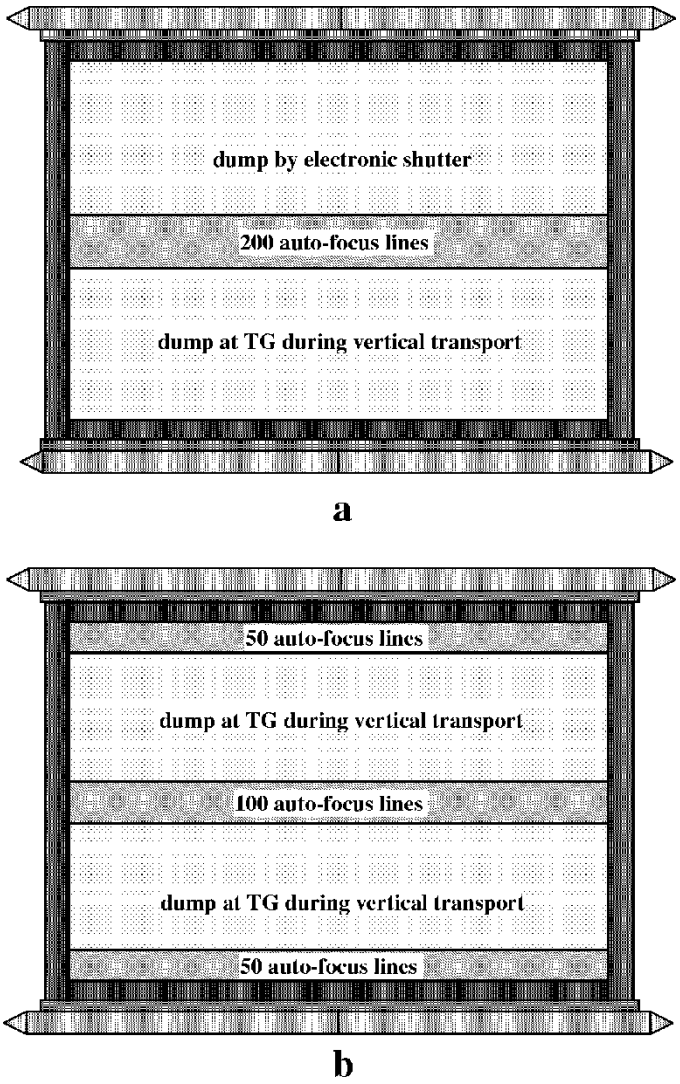

Fig. 8. Examples of auto-focus readout modes.

TABLE III
TYPICAL OPERATING CONDITIONS

Image clock swing (integration)	0V → 8V
Image clock swing (transport)	0V →11V
TG transfer clock swing	0V →11V
Horizontal clocks	4V → 9V
Reset gate	7.5V → 12.5V
p-well voltage (VPS)	6V
n-substrate voltage (VNS)	24V ≤ VNS ≤ 28V
electronic shutter pulse	≤ VNS + 10V
Typical V clock frequency	50kHz
Typical H clock frequency	25MHz

determines (together with the noise floor in dark and the amplifier noise) the dynamic range of the image. For professional applications, a linear dynamic range of at least 12 bits (72 dB) is required, "linear" implying here a deviation of less than 1% from the linear fit.

Highlight Handling: Efficient highlight handling through vertical anti-blooming is an essential requirement for imagers

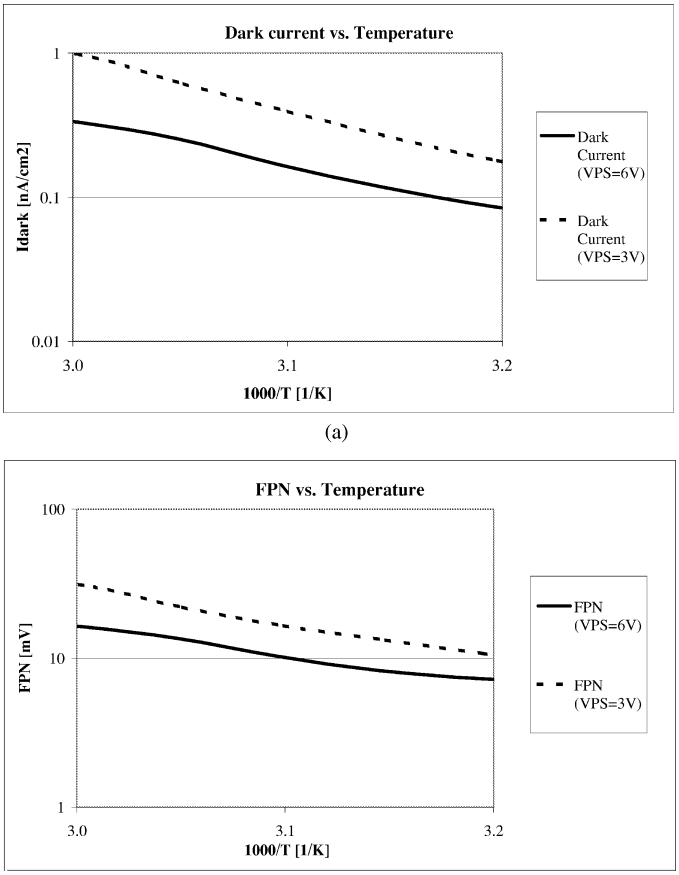

Fig. 9. Plot of (a) dark current and (b) FPN in dark versus temperature, for $\mathrm{VPS} = 6$ V and $\mathrm{VPS} = 3$ V.

for DSC cameras. The vertical npn structure shown in Fig. 2 can handle more than 1000 × overexposure without blooming.

Electronic Shutter: In this full-frame CCD sensor with a vertical n-p-n structure, all charge can be drained instantaneously to the n-substrate by setting all the image electrodes to the low level, and applying a pulse to the n-substrate. For the imager presented here, a 10 V positive pulse on the n-substrate during one line readout cycle is sufficient to completely empty all pixels.

Dark Durrent: A dark current level of 0.35 nA/cm^2 at 60 °C is measured under typical operating conditions, corresponding to a signal level of 50 electrons per pixel at 1/30 s exposure time.

Fig. 9 shows the dark current (in nA/cm^2) and the fixed pattern noise in dark (in millivolts) as a function of temperature between 40 °C and 60 °C (temperature axis shown as 1000/K) for the typical operating conditions $(\mathrm{VPS} = 6\ \mathrm{V})$, and for $\mathrm{VPS} = 3$ V. As can be seen, the dark current increases about a factor of two when decreasing VPS from 6 V to 3 V, since the electrical fields in the image pixel are increased, and since no pinning is present any longer under the "off" gates [8].

RGB Response: The RGB response of the imager is shown in Fig. 10. As can be seen, the metal-2 layer under the color filters ensures good pixel separation. This reduces the matrix correction required to obtain the correct color rendition. This largely compensates for the small loss in aperture by applying the metal-2 grid over the imaging array.

Angular Response: Lenses used in SLR cameras may have chief ray angles of up to 30° at the edge of the image. This

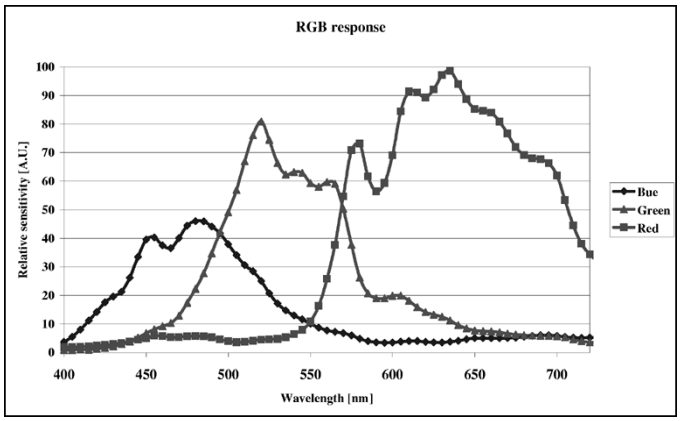

Fig. 10. RGB response.

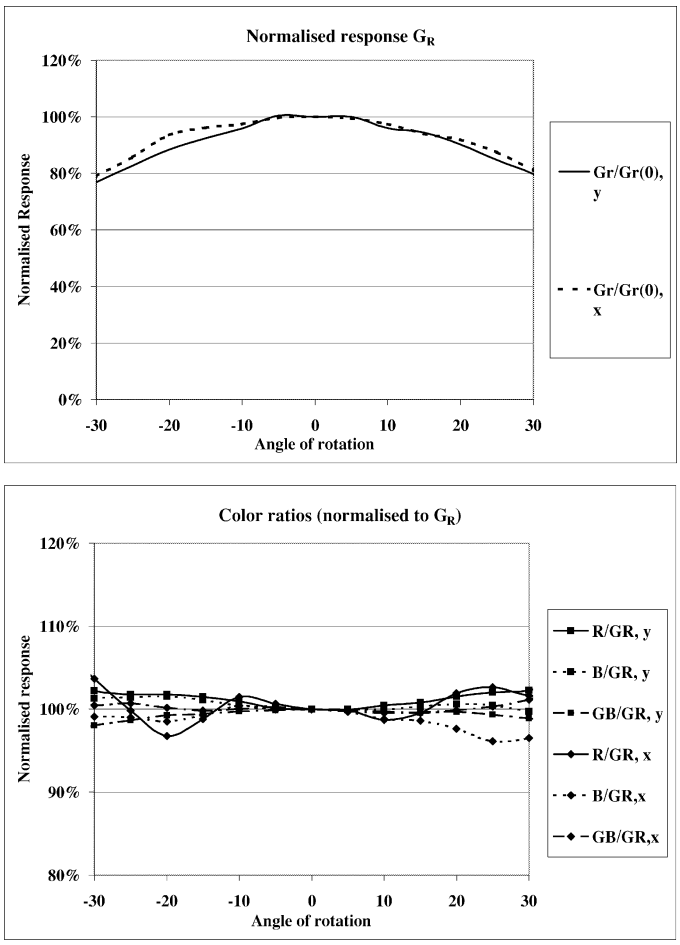

Fig. 11. Angular response measurement results.

requires an excellent angular response of the image pixels to avoid any color shading effects over the entire image.

Since this full-frame imager has an intrinsic high aperture of 80% (intrinsic = without microlenses), and since the stack height from color filter to silicon is only 3 μm, the response is not a strong function of the incident light angle. Interline CCDs and CMOS image sensors with intrinsic low fill factors and (especially for CMOS sensors) larger stack heights, require microlenses and thus are much more susceptible to this effect.

Fig. 11 shows the measured angular response for a the 9×9 μm^2 pixel, for illumination with white light. "X" means a rotation around the vertical axis, such that the light is directed to horizontally neighboring pixels across the p$^+$ channel stops. "Y" means a rotation around the horizontal axis, directing light to the vertically neighboring pixels at the other sides of the blocking gates. The four color planes for an RGB Bayer pattern are defined as (1) the blue pixels (B), (2) the red pixels (R), (3) the green pixels in the red rows (G_r), and (4) the green pixels in a blue rows (G_b). The top plot shows the response of the G_r signal as a function of rotation (x and y), normalized to "1" for perpendicular light. The bottom plot shows the change in color ratios (R/G_r, B/G_r, and G_b/G_r), again normalized to "1" for perpendicular light. The results not only show that the response decreases less than 20% over a 30° rotation angle, but also that the color ratios change less than 4%.

C. Imaging Array Evaluation

Linearity: Excellent system linearity is essential for reconstructing a color image from a CCD imager over a $\geq$ 12 bit dynamic range. The overall system to be considered for a CCD imager is the linearity from "photons in" to "mV out."

Fig. 12 shows a typical response (in number of electrons) of the four color planes as a function of integration time, for white light. The response from the blue curve shows that there is no blooming from "full" neighboring green pixels in the blue pixels. The saturation of the green pixels does not influence the blue response. Fig. 13 shows the deviation from the linear fit for these four responses. The deviation is well below $+/-1\%$ up to saturation, which is determined by the barrier to the vertical overflow drain. A linear charge capacity $(Q_{\rm lin})$ of 100 000 electrons is achieved, the maximum charge capacity $(Q_{\rm max})$ is around 120 000 electrons. The deviation at small signal levels is attributed to measurement inaccuracies.

Influence of Transport Clock Voltage and Frequency: The RC-times of the image clocks of large area CCD imagers are considerable, as the poly-silicon gates are only connected to the metal bus-bars at the left and right sides of the imaging array, spaced 36 mm apart. This implies that with increasing image clock frequency, the effective clock swing in the middle (left-right) of the imager will be reduced. Since this decreases the charge capacity during transport, charge mixing between vertically neighboring pixels would occur for large charge packets in the center of the imaging array.

The RC-times can be significantly reduced by adding metal strapping [6], but this would increase the number of process steps, and thus decrease the yield for these very large devices. An alternative solution is to use higher clock levels for the image clocks during transport, compared to integration. As shown in Table III, the integration voltage on the image electrodes is 8 V, while the transport clock swing is 11 V. At 50 kHz vertical transport frequency, this results in the linear performance as shown before in Fig. 12, indicating no transport loss occurs: even the largest charge packets obtained at 8 V integration voltage can be efficiently transported at 50 kHz vertical transport frequency with 11 V clock swing. If the transport clock swing is not increased, charge mixing will occur at 50 kHz transport frequency, as shown in Fig. 14. The response for G_r and B for the top 50

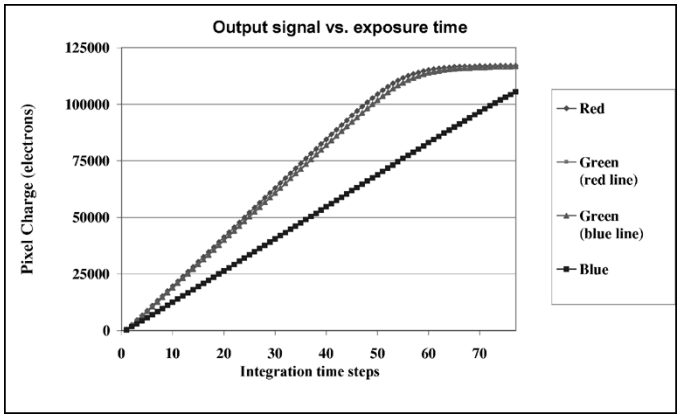

Fig. 12. Output signal per color plane as a function of exposure time.

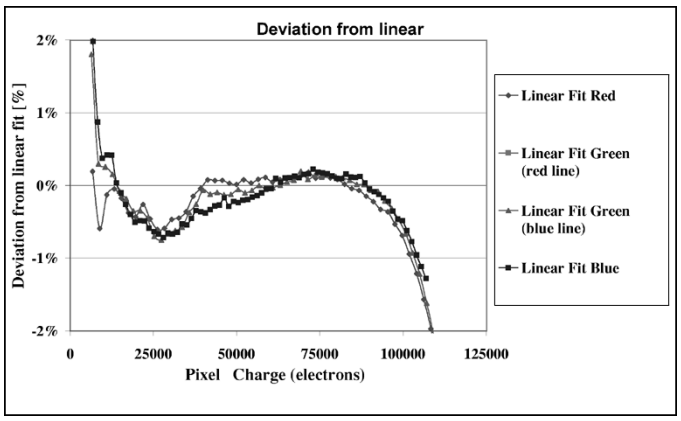

Fig. 13. Deviation form linearity at default sensor settings, as a function of exposure level.

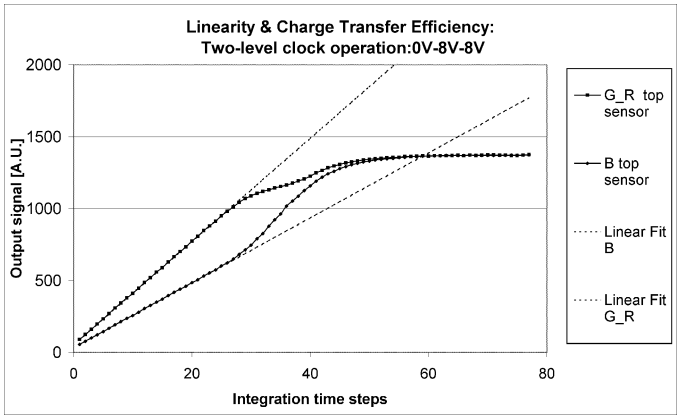

Fig. 14. Deviation from linearity caused by charge loss without use of three-level clocks.

lines of the imager as a function of exposure time, and the linear fit of this response for small signals, are plotted. It can be clearly seen that large G_r charge packets lose part of their charge to their smaller vertical neighboring packets B. As can be seen in Fig. 15, a similar effect occurs with three-level clocking if the frequency is increased from 50 kHz to 100 kHz.

However, there is a limit to increasing the transport clock swing: excessively high transport clock voltages will "pull" large charge packets closer to the interface; where charge then

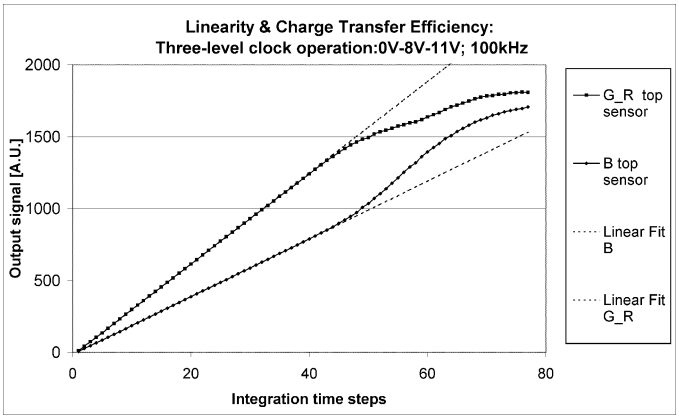

Fig. 15. Deviation from linearity caused by charge loss because of too high transport frequency.

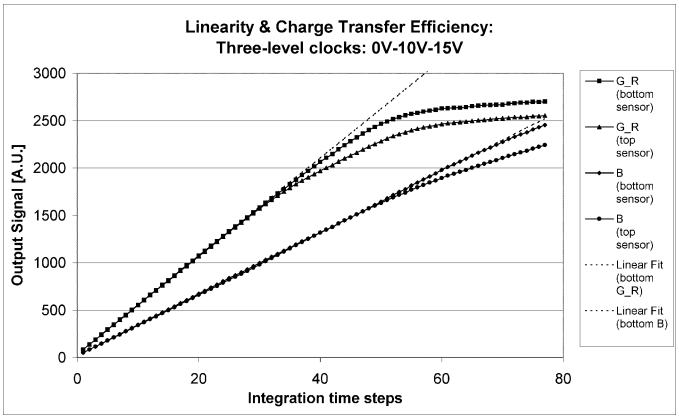

Fig. 16. Deviation from linearity caused by charge trapping at interface at too high transport clock level.

will be trapped. This is illustrated in Fig. 16. To increase the visibility of this effect, the integration voltage was increased to 10 V (to increase the maximum size of the charge packets during integration), and the transport swing was set to 15 V. The linearity was measured in the bottom 50 lines of the imager (only a few hundred transports to the readout register), and in the top 50 lines (about 10 000 transports to reach the serial register). Only the result for the "blue columns" are shown (B pixels and vertical neighbors G_r). As can be seen, large G_r charge packets from the top of the imager will lose part of their charge to interface traps. The effect starts at the same charge packet size (output signal 1700 A.U.) for "blue" as for "green" packets, implying no charge mixing occurs (from large green to small blue signals). The reason for this is that at the default VPS setting of 6 V, the Si-SiO_2 interface under the blocking gates is inverted with holes [9]. The electrons will recombine and are thus lost: this explains why the charge loss of the large packets will not influence the neighboring small packets. (It was experimentally verified that this charge was not lost to the substrate through the vertical n-p-n structure: changing the overflow barrier to the substrate by modifying the VNS voltage had no effect on the amount of charge loss.) However at lower VPS values (e.g., $\mathrm{VPS} = 3\,\mathrm{V}$), no hole inversion layer is present, and the trapped electrons are released, mixing during transport with following charge packets. In this case the charge lost by the large G_r pixels will be partially recovered by the B pixels. This can be observed in Fig. 17 where

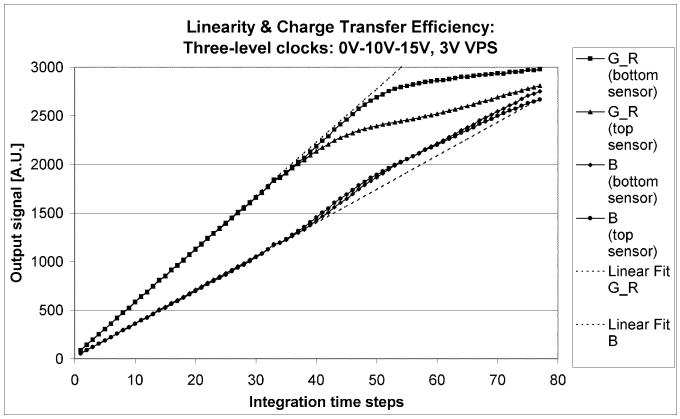

Fig. 17. Deviation from linearity caused by charge trapping at interface, at 3 V VPS voltage.

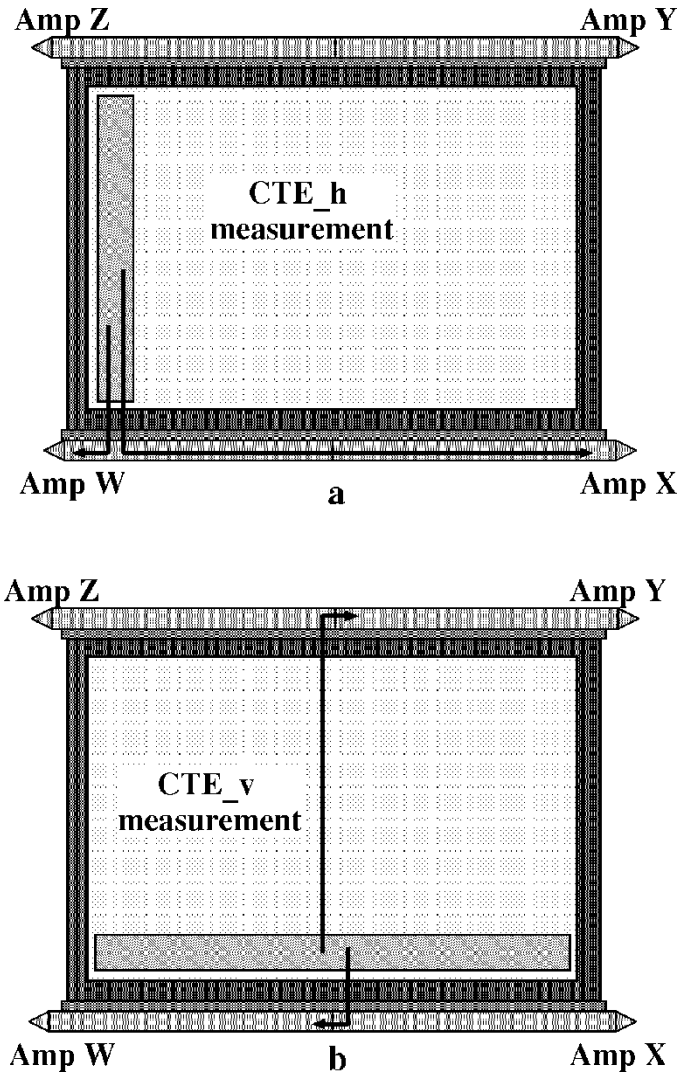

Fig. 18. Sensor areas used for measuring horizontal and vertical transport efficiency.

TABLE IV
COLOR RATIOS VERSUS TRANSPORT

CTE_H	readout through Amp W	readout through Amp X
Ratio B/G_b	5.341	5.342
Ratio G_r/R	1.765	1.764
CTE_V	readout through Amp W	readout through Amp Y
Ratio B/G_r	5.342	5.344
Ratio G_b/R	1.907	1.906

TABLE V
EVALUATION OF SUBSAMPLING EFFICIENCY

Color Ratio	full resolution	sub-sampled
B/G_b	5.50	5.49
B/G_r	5.61	5.61
B/R	9.97	9.95

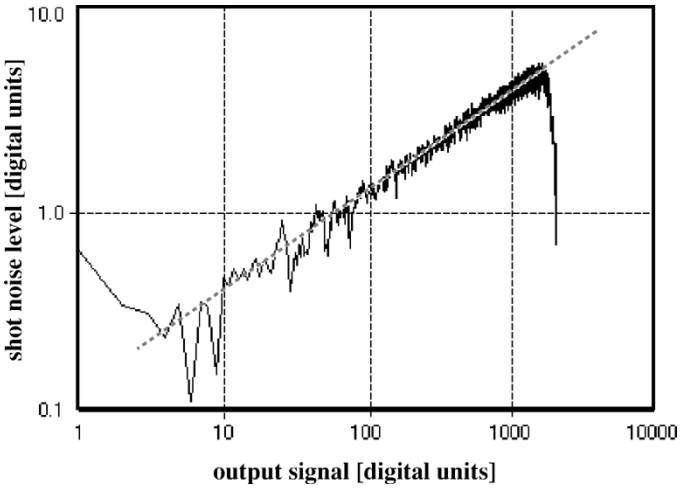

Fig. 19. Results of photon shot noise measurement.

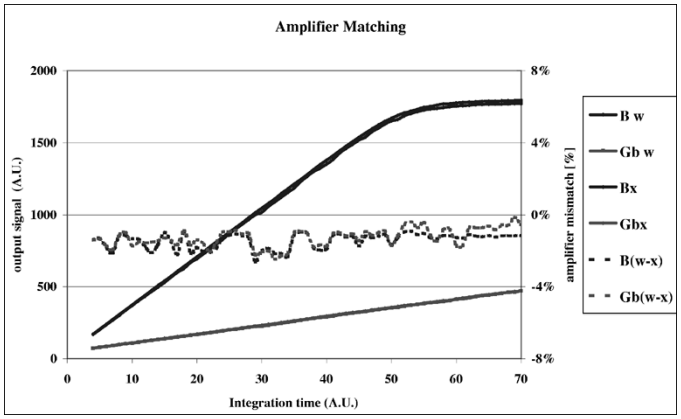

Fig. 20. Amplifier matching measurement results.

the Blue signal exceeds the linear fit as soon as the G_r pixels lose part of their charge.

The above theory was verified with 3-D electrostatic simulations. This showed that indeed at 15 V clock swing, large packets do reach the surface. At VPS $=$ 6 V, a hole inversion layer under the blocking gates was observed, which is not present at VPS $=$ 3 V.

TABLE VI
OVERVIEW OF LARGE-AREA IMAGERS

	11 M pixel CCD (this work)	**6 M pixel CCD** (previous work)	**16 M pixel CCD** (other vendor)	**2-M pixel CMOS** (other vendor)
Pixel count	4008×2672	3036×2024	4096×4096	1808×1120
Pixel size	$9\times9\mu m^2$	$12\times12\mu m^2$	$9\times9\mu m^2$	$15\times15\mu m^2$
Readout modes	single to 4-quadrants outputs	single to 4-quadrants outputs	single output	n.a.
Readout resolution	vert.sub-samp. option	full resolution only	full resolution only	n.a.
Instant electronic shutter	yes	yes	no	yes
Minimum full-resolution readout cycle	120ms	65ms	1200ms	180ms
Number of horizontal clock phases	3	3	2	(x)
Horizontal clock swing	5V	5V	12V	(x)
Maximum pixel frequency	4× 25 MHz	4× 25 MHz	15 MHz	12 MHz
Number of vertical clock phases	4	4	2	(x)
Vertical clock swing	11V	14V	10.5V	(x)
Vertical clock frequency	50kHz	50kHz	50kHz	(x)
Anti-blooming	vertical	vertical	lateral	through reset trans.
Maximum overexposure	≥1000×	≥1000×	≥200×	n.a.
Charge transfer efficiency	≥0.999 999 5	≥0.999 999	≥0.999 999	(x).
Signal-to-voltage conversion	$12\mu V/e^-$	$7.5\mu V/e^-$	$13\mu V/e^-$	$7\mu V/e^-$
Q_{lin}M	100 000	250 000	65 000	185 000
Dark current (60^oC)	300 pA/cm^2	300 pA/cm^2	450 pA/cm^2	5000pA/cm^2
Linear Dynamic Range (T=60^oC, exp.time=1/30 s)	75dB	78dB	73dB	64dB

(x) = not applicable

n.a. = information not available

Charge Transfer Efficiency: A classical method of measuring CTE is by observing the residual charge in the black reference columns (for horizontal CTE_H) and lines (for vertical CTE_V). However, this method assumes the first black reference lines and columns are perfectly "black" and requires a "perfect" step response in the off-chip electronics. charge transport efficiency can be more efficiently measured at application frequencies on high-resolution CCD imagers provided with RGB Bayer color filters and multiple outputs. When the sensor is illuminated with blue light, large "blue" charge packets (B) have very small horizontal (G_b) and vertical (G_r) neighbors. To measure the horizontal transfer efficiency, the color ratio in the left-most 100 columns of the imager is measured first when using Amp W ; the number of horizontal transport stages is negligible, Fig. 18(a). Next these ratios are measured for the same columns when using Amp X. Now about 10 000 horizontal transport stages are required. Any charge transport inefficiency would cause charge mixing, and thus reduce the color ratio. Similarly, the vertical charge transfer efficiency CTE_V was measured by comparing the color ratios in the bottom-most 100 rows, first using Amp W, next using Amp Y, as shown in Fig. 18(b). Table IV shows the measured color ratios. As can be seen, they hardly change. From these experiments, a horizontal and vertical charge transfer efficiency $\mathrm{CTE}_H = \mathrm{CTE}_V \geq 0.999\,999\,5$ was extracted. This implies a loss of less than 0.6% over the whole width or height of the sensor. Note that this method is also independent of any variation of the color response over the array, since the same image area is used for each set of measurements.

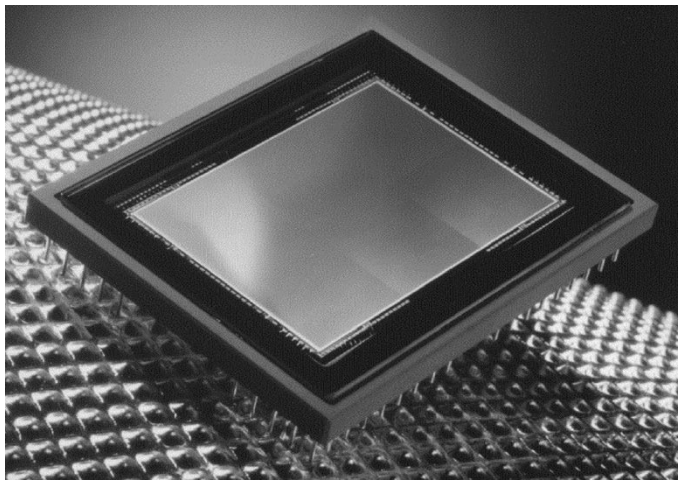

Fig. 21. Photograph of assembled CCD.

Fig. 22. Image obtained with 35-mm 11 M-pixel CCD. (Photo courtesy of Mosaic Imaging.)

Evaluation of Subsampling Efficiency: An efficient method to measure the subsampling performance consists in comparing the RGB response in full resolution mode and in monitor mode. The color ratios Green/Blue and Red/Blue should be identical in subsampled mode and in full-resolution mode. The sensor was illuminated with blue light (450 nm). With "perfect" subsampling, charge dump at the image to register transition should empty the pixels for 100%, and no charge mixing between the "dumped" and the "conserved" lines should occur. Any vertical charge loss of the large "blue packet" would increase the size of G_r, and thus influence the sensitivity ratios B/G_b and B/G_r. As can be concluded from Table V, the sensitivity ratios do not change between subsampling "off" and "on," implying no charge mixing or undesirable charge loss occurs. As long as the charge packets do not saturate, the measurement shows no influence of the size of the charge packets.

Photon Shot Noise Measurements: An alternative way to check the system linearity is by measuring the shot noise as a function of signal level. The process of converting incident photons to electron-hole pairs in an imager is characterized by photon shot noise; the noise level is equal to the square root of the number of generated (or collected) electrons. This basic physical phenomenon can be used to check the system linearity and noise floor.

The imager is illuminated with a grey scale ranging from "dark" to saturation. Two "identical" exposures are taken. Next a dark scene is taken with the same exposure time. The black level is then subtracted from both grey images, pixel per pixel. Next, both dark-offset corrected grey images are compared, pixel per pixel: for each pixel, the average level of the two exposures is calculated, and the deviation is measured. Finally, a plot is made (Fig. 19) showing for each average signal level (linear scale) the deviation (log scale): this is in fact the plot of photon shot noise versus signal level. A linear behavior on this lin-log scale as shown in Fig. 19 indicates a linear system response.

Amplifier Performance: The amplifier achieves 12 μV/electron conversion factor. The bandwidth is 110 MHz. The noise level, after CDS (correlated double sampling) processing is around 16 electrons.

Linear Dynamic Range: With 100 000 electrons Q_{lin}, 16 electrons amplifier noise and $\sqrt{50}$ electrons shot noise from the dark current (for 1/30 s exposure time at 60 °C, see above), a linear dynamic range of $20 \times \log(100\,000/\sqrt{(16^2+50)})$ dB $= 75$ dB is achieved.

Amplifier Matching: When using the option of high-speed readout through different outputs, it is important that the amplifiers (spaced more than 35 mm apart on the chip) are well matched. To check for possible differences in behavior,

the sensor was illuminated with monochromatic blue light and the response of the four color planes R, G_B, G_r, B was measured as a function of exposure time, first using amplifier W, a second time using the horizontally opposite amplifier X. Fig. 20 shows the response for the large B signal and for the small green signal in the same line G_B for both amplifiers. As can be seen, for both colors, the gain offset is constant, and less than 2% up to saturation. This can be easily calibrated and corrected in the camera system.

V. Comparison to Other Large Imagers

Table VI compares the performance of this new 11 M pixel imager with the previous 6 M device, and with CCD and CMOS devices supplied by other vendors.

As can be seen, the device presented here excels especially in linear dynamic range, pixel rate, and minimum readout time.

VI. Conclusions

A 35-mm 11 M pixel full-transfer CCD with multiple full-resolution and subsampled readout modes was presented. The device is compatible with a previously reported 6 M pixel CCD. Very high transport efficiency, good output amplifier matching and flexibility of vertical subsampling and a wide angular response offer important application advantages. The combination of low dark current and high charge capacity result in a linear dynamic range of 75 dB.

Fig. 21 shows a photograph of the assembled 11 M pixel CCD imager, Fig. 22 gives an image obtained with this device.

Acknowledgment

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Jan T. Bosiers (M'85–SM'02) was born in Mortsel, Belgium, in 1956. He graduated as an Electronic Engineer from the Catholic University of Leuven, Belgium, in 1980.

From 1980 to 1984, he was a Research Scientist at the ESAT Laboratory of the Department of Electronic Engineering, at the University of Leuven, where he developed high-resolution linear CCD imagers. From 1985 to 1986, he was a Consulting Engineer at the U.S. Naval Research Laboratory in Washington, D.C., working on R&D of deep-depletion, backside illuminated CCDs for detection of UV and X-ray radiation. Since October 1986, he has been with Philips in Eindhoven, The Netherlands. Since April 2002, he has been with DALSA B.V., Eindhoven. He has worked on the research, development, and project management of CCD imagers for consumer and medical applications, and is currently R&D Manager at DALSA B.V. He has contributed to several CCD papers presented at IEDM meetings and published in the the IEEE Transactions on Electron Devices.

Mr. Bosiers received the first "Walter Kosonocky Award" honoring the best paper on electronic imaging for the years 1998–1999, for his 1998 IEDM contribution on FT-CCDs for digital camera applications.

Bart G. M. Dillen was born in Geldrop, The Netherlands, on October 11, 1958. He received the Ingenieur Diploma in electronics from the Eindhoven Technical College, Eindhoven, The Netherlands.

From 1982 to 1989, he was a Research Scientist at the Philips Research Laboratory in Eindhoven where he worked on characterization and design of CCD imagers. From 1989 to 1996, he was a Development Engineer at Philips Medical Systems, Best, The Netherlands, working on R&D of medical X-ray cameras. Since August 1996, he has been working at Philips Semiconductors, Eindhoven. In the Image Sensors Group he has worked on the research, development, and project management of CCD imagers. Since April 2002, he has been Project Manager for CCDs for professional and prosumer applications at DALSA B.V., Eindhoven.

Cees Draijer was born in Maasland, The Netherlands, in 1967. He received the Ingenieur Diploma in applied physics from the Eindhoven Technical College, Eindhoven, The Netherlands, in 1993. In 1997 he received the M.S degree in applied physics from the Eindhoven University of Technology.

From 1997 to 2002 he was a Research Scientist at Philips Semiconductors Image Sensors, Eindhoven, where he worked on simulation and design of CCD imagers. Since April 2002, he has been with DALSA B.V., Eindhoven.

Agnes C. Kleimann was born in Heemskerk, The Netherlands, in 1962. She received the Ingenieur Diploma in physics from Dordrecht Technical College, The Netherlands, in 1986.

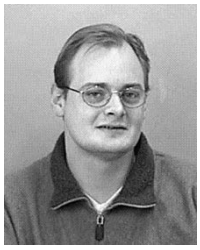
In 1986, she joined Philips Semiconductors Image Sensors. Her work comprised CCD device and process modeling, and evaluation of CCD image sensors. Since April 2002, she is with DALSA B.V., Eindhoven, the Netherlands.

Frank J. Polderdijk was born in Biervliet, The Netherlands, in 1964. He received the Ingenieur Diploma in electronics from the Technical University, Eindhoven, The Netherlands.

From 1990 to 1998, he was a Development Engineer at Philips Digital Video Systems, Breda, The Netherlands, working on development of HDTV broadcast cameras, medical X-ray cameras, and several other OEM camera systems. Since July 1998, he has been working at Philips Semiconductors in Eindhoven, the Netherlands. In the Image Sensors Group he has worked on the development of DSC applications and application support of CCD imagers for professional and prosumer applications. Since April 2002, he has been with DALSA B.V., Eindhoven, the Netherlands.

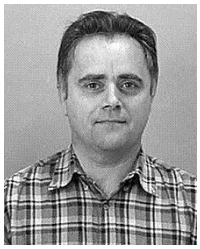
Marc A. R. C. de Wolf was born in Schiedam, The Netherlands, in 1968. He received the Ingenieur Diploma (M.Sc.) in technical physics at Delft University of Technology, and a Designer degree in electronics at University of Twente, The Netherlands.

From 1997 to 2001, he was a Development Engineer on video-processors and tuners at Business Line RF-Products, Philips Semiconductors Nijmegen, The Netherlands. Since March 2001, he has been working at Philips Semiconductors, Eindhoven, The Netherlands. In the Image Sensors Group, he has worked on the research, development, and project management of CCD imagers for professional and prosumer applications. Since April 2002, he is with DALSA B.V., Eindhoven.



Wilco Klaassens was born in Avenhorn, The Netherlands, in 1969. He received the Ingenieur Diploma in organic chemistry from Alkmaar Technical College, Alkmaar, The Netherlands, in 1993.

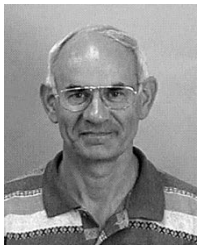
From 1995 to 1999, he was involved in research on soft-magnetic materials for SVHS magnetic heads and thin film heads for tape streamer device at the Philips Research Laboratory, Eindhoven, The Netherlands. Since 1999, he has been a CCD Technologist at Philips Semiconductor Image Sensors, Eindhoven. Since April 2002, he is with DALSA B.V., Eindhoven.



Albert J. P. Theuwissen (SM'95–F'02) was born in Maaseik, Belgium, on December 20, 1954. He received the degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1977. His thesis work was based on the development of supporting hardware around a linear CCD image sensor. He received the Ph.D. degree in electrical engineering in 1983. His dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

From 1977 to 1983, his work at the ESATLaboratory of the Catholic University of Leuven focused on semiconductor technology for linear CCD image sensors. In 1983, he joined the MicroCircuits Division of the Philips Research Laboratories, Eindhoven, The Netherlands, as Member of the Scientific Staff. Since that time he was involved in research in the field of solid-state image sensing, which resulted in the project leadership of SDTV- and HDTV-imagers. In 1991, he became Department Head of the Imaging Devices division, including CCD as well as CMOS solidstate imaging activities. He is author or coauthor of many technical papers in the solidstate imaging field and issued several patents. He is member of editorial board of the magazine *Photonics Spectra*. In March 2001, he became part-time Professor at the Delft University of Technology, the Netherlands, where he teaches courses in solid-state imaging and coaches Ph.D. students in their research on CMOS image sensors. In 1995, he authored a textbook *Solid State Imaging with Charge Coupled Devices*.

Dr. Theuwissen was a member of the International Electron Devices Meeting paper selection committee in 1988, 1989, 1995, and 1996. He was co-editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES Special Issues on SolidState Image Sensors, May 1991 and October 1997, and of *IEEE Micro* special issue on Digital Imaging, November/December 1998. He acted as general chairman of the 1997 IEEE International Workshop on Charge-Coupled Devices and Advanced Image Sensors. He is member of the Steering Committee of the aforementioned workshop and founder of the Walter Kosonocky Award, which highlights the best paper in the field of solid-state image sensors. During several years he was a member of the technical committee of the European Solid-State Device Research Conference. Since 1999 he is a member of the technical committee of the International Solid-State Circuits Conference. For the same conference he is acting as vice-chair in the European ISSCC Committee and member of the overall Executive Committee. In 1998 he became an IEEE Distinguished Lecturer. He is a member of SPIE.



Herman L. Peek (M'79) was born in Haalderen, The Netherlands, in 1942. He received the Ingenieur Diploma in physics from Eindhoven Technical College, Eindhoven, The Netherlands, in 1969.

He joined the Semiconductor Research Group of Philips Research Laboratories, Eindhoven, in 1964, where he worked on MOS technology, silicon epitaxy, and silicon vidicon devices. Since 1973, he has been working in the CCD Research Group, where he has been responsible for the development of frame-transfer solid-state image sensor technology. He is currently a Philips Semiconductors Fellow. From 1973 to 1983, he also worked on the development of EEPROM technology.

Hein Otto Folkerts was born in the 1967. He received the M.Sc. degree in 1991 at the University of Groningen, The Netherlands, with experimental physics as main subject. In 1996, he received the Ph.D. degree from the University of Groningen in the field of atomic physics on electron transfer in ion-molecule collisions.

In March 1996, he started working at Philips Research Laboratories, Eindhoven, The Netherlands, in the group of Albert Theuwissen on Device Physics of CCD image sensors, which in 1999 became part of Philips Semiconductors. Currently, he is working within Philips Semiconductors Imaging on CMOS image sensors, heading the Imaging Technology Development Group.