

## Chapter 3.3

# CMOS IMAGE SENSORS FOR AMBIENT INTELLIGENCE

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**Abstract:** Ambient Intelligence (AmI) hinges on three key technologies: ubiquitous computing, ubiquitous communication, and intelligent user-friendly interfaces. In order for there to be intelligence and communication of relevance to people, sensor inputs are essential. One of the most versatile and, in our estimation, crucial of all possible inputs is the image sensor. To fulfill the dream of AmI and to assure widespread adoption of the image sensor, one must address the following criteria: cost, power, versatility, and adaptability. We will present an overview of the current state of the image sensor and indicate some of the ways in which hardware designers might meet the challenge of addressing these criteria.

**Key words:** image sensors

## 1. INTRODUCTION

Ambient Intelligence (AmI) relies on inputs from the external world to enhance, improve, facilitate, and to secure the life of humanity. Applications range from automotive (collision avoidance, smart highways),<sup>1,2</sup> security (biometrics, fingerprint recognition for payments in grocery stores, facial recognition for border control, Nigerian scam baiters),<sup>3,4</sup> medical (assisted living, diagnostics),<sup>5,6</sup> hazardous operations (mine sweeping, smart buildings),<sup>7</sup> social (video conferencing, museums),<sup>8</sup> cultural (sports),<sup>9</sup> gaming (virtual reality),<sup>10</sup> to the esoteric such as satellites (star trackers).<sup>11</sup> Inputting the external stimuli will very often involve visual cues and hence the primacy of the image sensor.

It was in the mid eighties that solid-state image sensors replaced the classical imaging tubes in video applications. Although the first papers on solid-state imaging were published in the sixties, it took almost two decades before solid-state imagers could make any inroads into the consumer market. The main reason for this long design-in period was the lack of a mature technology to fabricate the imaging devices. Photographic equipment has recently gone through the same process as the imaging tubes did in the past. The cost-quality ratio of solid-state image sensors is becoming so attractive that they pop up in many new, emerging markets that are the forerunners of AmI, like mobile imaging and automobiles. The AmI era will be the ultimate mass market for solid-state imagers.

Today's image sensors are based on two technologies: CCDs (Charge-Coupled Devices),<sup>12,13</sup> which are made in a dedicated semiconductor process, and CMOS imagers (Complementary Metal-Oxide-Semiconductor), which are produced in a standard semiconductor process.<sup>14,15,16</sup> For AmI applications, cost and power consumption are the two most crucial characteristics. Therefore, it should not be surprising that CMOS with their cost advantages, when produced on a large scale and their inherent power advantages over CCDs is believed to be the technology of choice for AmI.

The goal of this paper is to provide an overview of the state of the art in CMOS sensors, and provide a roadmap for future developments. The layout of the paper is as follows. In the first section, the overall underpinnings of image sensors are presented. The next section involves global power considerations and on-chip processing, followed by a section on the analog chain. The last section highlights the myriad possibilities that can be addressed by novel designs to solve unique issues. We conclude with a summary and outlook for imager design and potential.

## **2. IMAGE SENSOR ARCHITECTURE**

Imagers can be built up one-dimensionally (e.g. facsimile), but most of them are constructed in a two-dimensional configuration (e.g. video, automotive, mobile).

### **2.1 Basics of CMOS imagers**

A CMOS XY-addressable imager is a matrix of photodiodes, each of which is provided with a MOS transistor acting as a switch. This setup is shown schematically in Figure 3.3-1. The basic structure of a unit cell consists of a photodiode connected to the output by means of a sensing line. To convert the two-dimensional spatial information into the serial stream of

electrical signals, electronic scan circuits are added to the device to address all pixels in a sequential mode and to read out their information. This addressing feature forms the basic operation of the device. At the beginning of a new field, the vertical scan circuit is activated. Suppose that the first row of pixels is selected. This is done by setting a high DC voltage on all gates of the MOS switches of this first row. Next, the horizontal scan circuit selects the pixels on one particular column by scanning its own outputs using a single high DC output, while all others are at a low level. This combination of one output of the vertical scanner and one output of the horizontal scanner at a high level and all the others low, selects one single pixel from the two-dimensional matrix. This pixel can be emptied and dump its information into the output stage. Immediately after this action, the pixel can be reset and restart an integration. The neighboring pixel will then be addressed and read out.

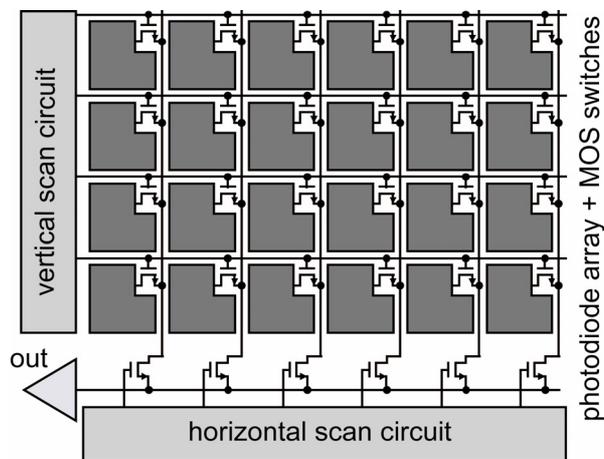


Figure 3.3-1. The basic architecture of a CMOS XY addressable imager with an array of passive pixels.

The XY-addressed imager with passive pixels (the simple photodiode) is limited in its performance due to the relatively high levels of noise and fixed-pattern noise (FPN). FPN is the variation in output between various pixels given the same input. In a perfect imager, each pixel produces the same output given the same input, but in actual image sensors, the output of each pixel is different. These differences are partly caused by the small capacitance of the photodiode, which is connected to the large readout capacitance of the sensing line. A small amplifier can be added to every pixel to overcome these noise sources. A source-follower stage (amplification in the charge domain) is constructed within every single pixel,

and with appropriate correlated-double sampling circuitry (see section 4) on the column buses, the noise and the fixed-pattern noise can be limited.

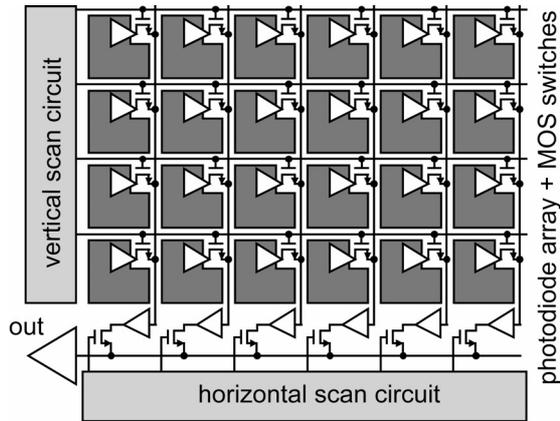


Figure 3.3-2. The basic architecture of a CMOS XY addressable imager with an array of active pixels.

The architecture of the Active Pixel Sensor (APS) is very similar to the Passive Pixel Sensor (PPS). Figure 3.3-2 shows this architecture. In both cases, after selection of the appropriate pixel by the scan circuitry, the information is read from the pixel: the charge is transported from the photosensitive area towards a floating diffusion amplifier by means of the transfer gate. The driver of the source follower stage (the amplifier in the pixel) is implemented in the pixel itself; the load of the source follower is common for all pixels on a column.

Compared to the PPS, the overall noise and fixed-pattern noise performance of the APS sensors is improved by at least one order of magnitude.

## 2.2 Pixel configurations

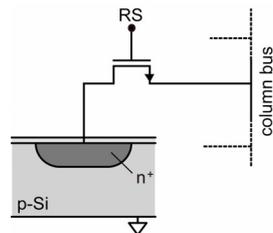


Figure 3.3-3. Basic configuration of a passive pixel.

The *passive pixel* is very simple in construction (see Figure 3.3-3): 1 photodiode, 1 transistor and 2 interconnects. The pixel is characterized by a large fill factor, but unfortunately also by a large noise level. After addressing the pixel by opening the row-select transistor (RS), the pixel is reset along the column bus and through RS.

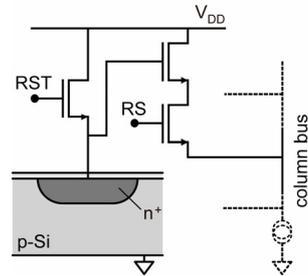


Figure 3.3-4. Basic configuration of an active 3T pixel.

The *active pixel* has an amplifier within every pixel (see Figure 3.3-4). The amplifier is configured as a source follower: the driver of the source follower is located in the pixel itself, the load of the source follower is placed on the column bus, but physically out of the focal plane. The two other transistors in the pixel are used for addressing (row-select or RS) and resetting the pixel (RST). Every pixel has 1 photodiode, 3 transistors, and 4 interconnects.

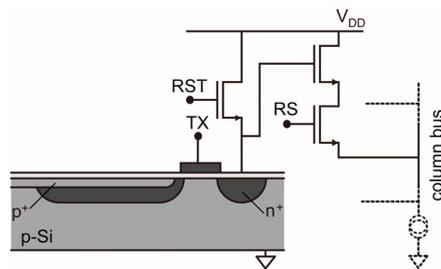


Figure 3.3-5. Basic configuration of a pinned-photodiode pixel.

After addressing a pixel, its actual video level is sensed by the source follower and fed to the column bus, next the pixel is being reset, and a new integration cycle can start. This APS pixel has become very popular in CMOS image sensors, because it solves or mitigates many of the noise problems. Unfortunately, in the configuration shown, it still suffers from a large reset noise component. This drawback is solved in the pixel



### 3. POWER

Focusing on ambient intelligence applications of the CMOS image sensor, low power is, besides cost, certainly the main issue. Considering the power distribution inside a camera, it makes little sense to consider only the pixel-level power consumption. Figure 3.3-7 depicts the power dissipation for a QCIF (176 x 144) and VGA (640 x 480) CMOS image sensor, both operating at 60Hz frame rate with Analog to Digital Converters (ADCs). It is clearly shows that the majority of the power is actually not consumed in the pixel array. I/O, color signal processing, and ADC totally consume more than half of the power. Therefore, it is important to investigate the power issue in these components.

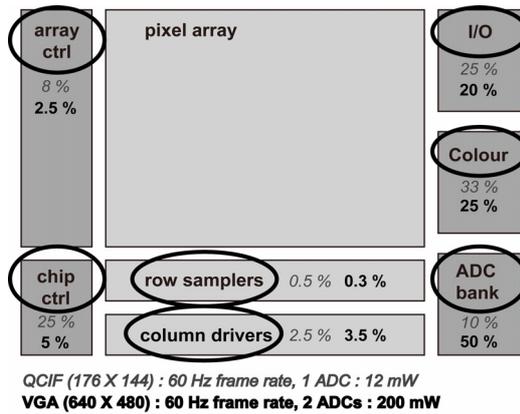


Figure 3.3-7. CMOS image dissipation for a QCIF and a VGA pixel.

#### 3.1 Power consumption in the signal processing unit

The signal processing can always be divided in two parts: analog signal processing and digital signal processing. In a CMOS image sensor, analog signal processing is essential to achieve high signal-to-noise ratios (SNR), and especially to minimize pixel and column Fixed Pattern Noise (FPN). The digital part normally takes care of the remaining image processing procedures, e.g., color interpolation and correction, white balancing, aperture correction.

After analog processing (see section 4), the video signal is converted to a digital signal by the ADC. Comparing with the analog part, the image digital signal processing certainly consumes much more power due to the added and multifaceted functionality. At the moment digital image processing units are mostly designed for photography applications<sup>17,18</sup>, i.e.,

color imaging. The digital signal processing that is necessary to correct the various problems is so complex, that the corresponding algorithms can even vary from pixel to pixel within one sensor.<sup>19</sup> In addition, due to this complex functionality, besides the power issue, the cost increases and these sensors are not very suitable for widespread AmI applications.

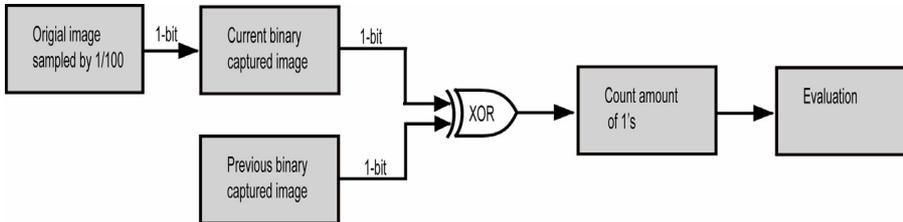


Figure 3.3-8. Block diagram of the algorithm for a low-power motion detection sensor.

Fortunately, in many cases, color processing is not necessary for AmI. Therefore, it is critical to develop an application-specific signal processing (ASSP) design, like in, for instance, motion detection, edge detection, or 3D detection (of interest in, for example, virtual reality), to acquire a simplified structure and reach the ultra-low power consumption needed. As a good example, researchers recently implemented a camera processor design using a CMOS image sensor especially for motion detection.<sup>20</sup> This is definitely an important application in ambient intelligence: to realize automatic inspection of environmental surroundings and detecting changes that are introduced. Figure 3.3-8 shows the block diagram of the proposed algorithm.

Traditionally, in order to detect motion, a previous image needs to be stored and compared with the current image. This leads to the need for a large memory and increased computing power during the required signal processing. In essence, the image data bit width used for comparison decides the power consumption. The novelty in this algorithm design is to choose only the most significant bit instead of all the data bits to make the comparison while not losing accuracy. The image signal processing unit as reported, includes an embedded microprocessor (ARM) and several hardwired modules using pseudo Advanced Microprocessor Bus Architecture (AMBA). Together with a power management block, which controls the system clocks by software, a reduction of 1/3 in overall power consumption can be achieved.

Even though the image processing functions are normally realized in the digital domain, the argument exists, that because digital processing require high resolution data, which may lead to a bigger chip size, and most of all, more power consumption. Therefore, there are designs<sup>21</sup> and products<sup>22</sup> to

integrate most fundamental signal processing before the ADC. Figure 3.3-9 is the functional block diagram of one of such products, OV7640 color CMOS VGA CameraChip from Omnivision Technology. Without a DSP unit, the only digital domain components are output formatter and the I/O circuit. Comparing with Figure 3.3-7, the same VGA resolution (640 x 480) with a dual ADC configuration is reported to use only 40mW active power (30fps) including the I/O power. Even considering the lower operation speed, dramatically reduced power consumption is seen.

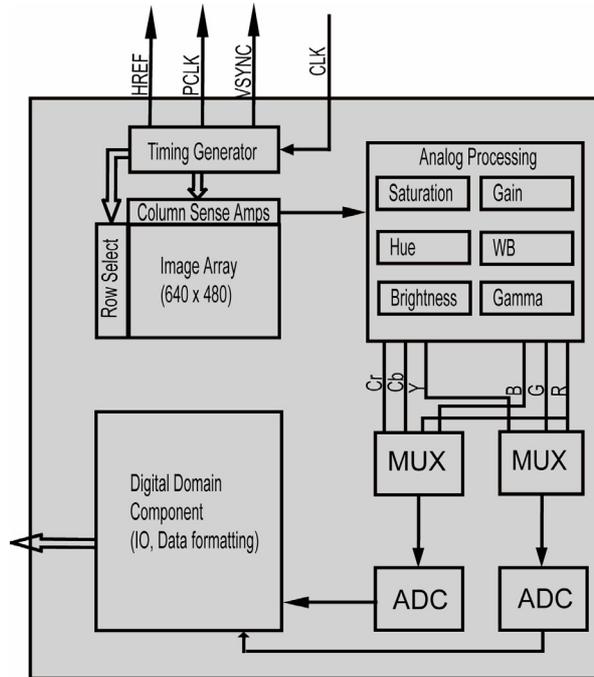


Figure 3.3-9. Functional block diagram for OV7640 VGA CameraChip.

With an application-specified processing unit design, power consumption in signal processing unit can be optimized and reduced further. Moreover, there are still quite a few strategies for power reduction in the DSP unit, e.g., dynamic voltage and frequency scaling, and resource hibernation. A lot of work is being carried out especially concerning power issues in processor design, both at the hardware and software level.<sup>23</sup> Also, due to the simpler functionality desired by ambient intelligence applications, further power reduction can be achieved by shifting the processing procedures from the digital to the analog domain. By doing this, the well-established low power analog circuit design techniques can also play a role.

### 3.2 Power consumption in the I/O unit

The I/O circuitry in a CMOS image sensor is another power-hungry component. It contains all the input and output control signals, such as clock, reset, and video output signals (analog/digital). For standard photography, a CMOS image sensor, e.g., a typical VGA resolution sensor has more than 30 I/O pins (8-bit RGB output formats).<sup>22</sup>

In order to adjust output current according to different loading needs, driving circuits such as buffers and amplifiers are needed for video output ports. Unfortunately, the downscaling of the technology leads to a reduced on-chip capacitance, while the off-chip capacitance remains the same. Therefore, the driving ability of the I/O unit becomes extremely important; and, as the consequence, higher power consumption is expected.

To achieve a low power design, the most straightforward method is to limit the amount of I/O. By doing this, the number of bits on the system-bus can also be limited, which results in a significant reduction of power dissipation due to its high switching activities and large capacitive load.<sup>24</sup>

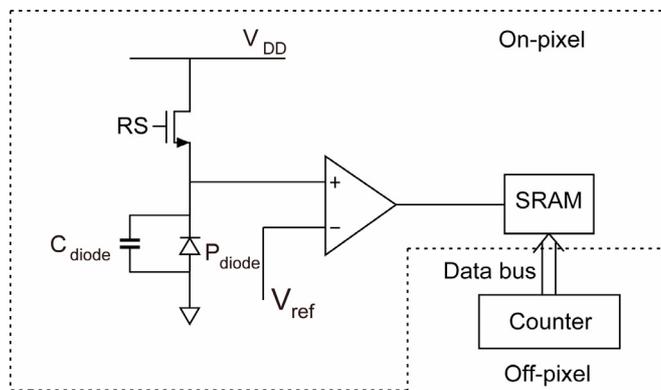


Figure 3.3-10. Pixel Structure of the on-pixel PWM ADC design.

For example, a number of pixel parallel ADC circuits have been reported based on a Pulse Width Modulation (PWM) scheme.<sup>25</sup> A similar design with on-pixel ADC based on PWM is reported.<sup>26</sup> Figure 3.3-10 is the pixel structure of this design. The main scheme of PWM remains the same. The difference of this design is that the on-pixel 8-bit memory can be reconfigured as a 4-bit counter. Therefore, the global data bus lines are also reduced by half. During integration, the in-pixel 4-bit counter generates the 4 MSB with respect to the video signal; an array-based off-pixel counter generates the 4 LSB based on the same video signal. Immediately after integration, the on-pixel 4-bit counter is configured back as an 8-bit memory.

By transferring the 4 LSB video signals from an off-pixel counter, the on-pixel memory holds the complete 8-bit digital video signal. Then, a special time multiplexing strategy is used to readout 8-bit data through the 4-bit bus. Therefore, the whole integration and readout phase can be handled with a 4-bit system bus. Logically, the power consumption due to system bus is reduced.

However, unless much less data is required at the output, for the same amount of data, the technique of limiting I/O may not produce the results wanted. Sometimes, the problems are just shifted downstream. Even though the amount of I/O is reduced by half, the switching speed may need to be doubled and extra circuits may need to be added in the pixel or in the ADC, which certainly leads to extra power consumption. Also other effects e.g. fill-factor, and ADC speed may be hurt because of it. Obviously, a careful trade-off is necessary.

In other words, the most efficient method for power saving is still an application-specified design, both for the signal processing unit and the I/O unit. Particularly for the AmI applications, since an ordinary digital video signal, e.g., 8-bit RGB data is not compulsory; a smaller number of I/O ports becomes decidedly more attractive. If a detection functionality is desired, for example, then a single output 'Yes' or 'No' may just be enough. Theoretically, the power consumption from the I/O unit is then optimized.

## **4. ANALOG SIGNAL PROCESSING IN CMOS IMAGERS**

### **4.1 Introduction**

The analog signal processing chain is an important component of a CMOS image sensor. First of all, the quality of this processing chain determines, together with the properties of the pixel array, the quality of the sensor. Second, a significant part of the total power of the image sensor is consumed in the analog signal processing, as is depicted in Figure 3.3-7.

The analog signal processing chain of a conventional CMOS image sensor can generally be divided into 3 parts, as is depicted in Figure 3.3-11.<sup>27</sup> The front-end of the chain is formed by the in-pixel readout transistor, which consists of only one source follower, as discussed in section 2.2 of this paper. To minimize the in-pixel area overhead, the source follower is usually of minimum size. As a result, it has a very high 1/f noise, particularly in modern deep-submicron CMOS processes. This 1/f noise cannot be decreased without fundamental changes to the processes, and usually therefore limits the overall quality of the processing chain.

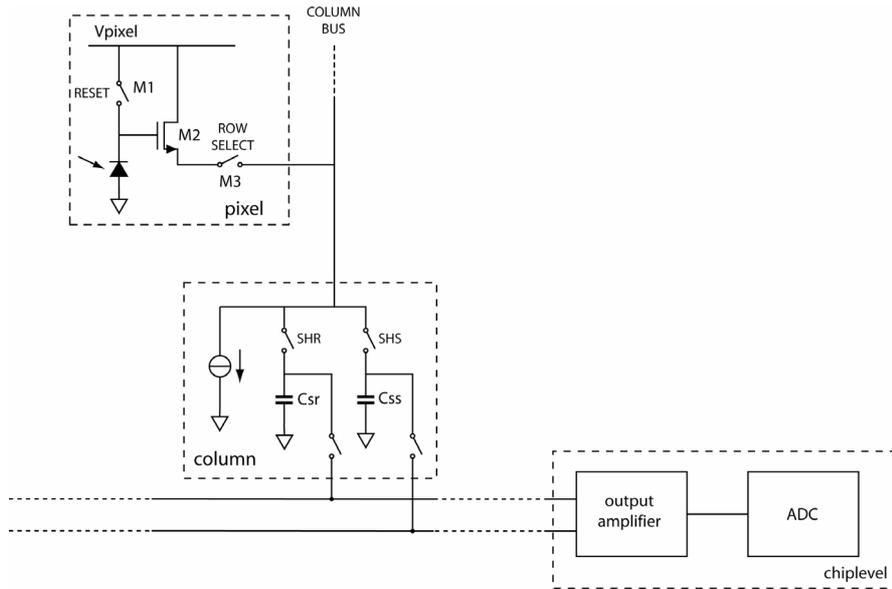


Figure 3.3-11. Overview of the analog signal processing chain of a CMOS imager.

The second stage of the chain is the column-level circuitry. This is a row of circuits situated below the imaging array, which is connected to one row of the imaging array at a time. The column circuit biases the in-pixel source-follower and samples both the pixel output signal and its offset. These voltages are stored on capacitors. Although many of these column circuits operate in parallel on a row of pixels, the combined power consumption of the first two stages is quite low. The reason for this is that in a conventional design, the column circuits are switched on only a small fraction of the (line) time.

The last stage of the analog signal processing chain consists of a central output amplifier and an A/D converter. The output amplifier reads out the column-level capacitors. By subtracting the capacitor voltages of each column circuit, a Correlated Double-Sampling (CDS) is performed, thus removing offset and noise. Since only a single output amplifier is used, it reads out the row of column circuits at high speed. Sometimes, an Automatic Gain Control (AGC) is added to the stage to decrease the necessary dynamic range of the A/D converter connected to the output of the amplifier. This A/D converter has usually a speed of 10-40 MSPS and a resolution of 8-12 bits. A pipeline or two-step architecture is commonly used for the ADC. The combination of output amplifier and ADC consumes most of the power in the analog signal processing chain, since it has to run at high speed, thus requiring high bandwidth circuits that consume a lot of power in order to be low noise.

In order to apply image sensors successfully in ambient intelligence, two aspects are of key importance. First and foremost, the power consumption of the imager has to be decreased as far as possible. Second, there should be a choice of output quality depending on the situation, i.e., it should be possible to adjust the necessary quality versus required power consumption dynamically. This has its impact on the analog signal processing chain, as will be shown in the next paragraphs.

## 4.2 Analog signal processing topology for minimum power consumption

Since most of the power of the analog signal processing chain is consumed in its ADC, efforts to minimize power should be focused on this part. Although there is a lot of research on optimizing the power consumption of general-purpose ADCs, imager read-out chains differ in one fundamental aspect: in an imager, several slower ADCs can be put in parallel without needing extra power in order to parallelize the signal path, as with a single-input general-purpose ADC. In recent years, research has been done on alternative signal processing chains, where the ADC is moved towards the front-end of the read-out. Several CMOS imagers were reported with a column-level ADCs<sup>28,29,30</sup> or even pixel-level ADCs.<sup>31,32</sup> Some advantages of this approach are obvious, such as a possibility for high-speed read-out and/or very high-resolution imagers. However, how these different topologies compare on power efficiency is less obvious.

Although it is difficult to make an accurate comparison between the different topologies without designing them, some estimation can be made. Without regarding to any specific ADC architecture, a fundamental aspect of analog circuitry is that voltage amplification is needed. The most basic circuit that delivers a gain is an inverting amplifier stage (Figure 3.3-12), loaded by an identical stage. If we regard only the transistor and consider its load resistor ideal, its bandwidth is determined by its transconductance ( $g_m$ ) and its parasitic capacitances, while its gain is determined by its transconductance and its output resistance. To maximize the power efficiency, it is therefore best to maximize the amount of transconductance the transistor can deliver for a given bias current. This means that the transistor has to be biased in weak inversion, where the ratio of transconductance to the bias current is maximum (typically around 25). This operation in weak inversion puts a lower limit on the  $W/L$  sizing of the transistor, which in turn determines the parasitic capacitance of the transistor. Therefore, if we choose to operate the transistor in weak inversion, there is a fixed relation between the transconductance and the

parasitic load capacitance, and therefore the bandwidth does not depend on the bias current.

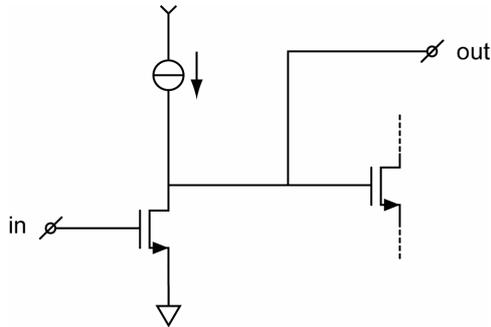


Figure 3.3-12. Basic amplifier configuration with one transistor.

A simple computer simulation of the circuit in Figure 3.3-12 in a  $0.18\mu\text{m}$  CMOS process shows that the mentioned bandwidth is around 15 MHz. This figure is of course an upper limit to what should be the process' capability; in particular, in a real amplifier the capacitive load is probably higher. When a chip-level ADC is used, its speed should be at least 10MSPS for a VGA resolution sensor. As a result, the transistors in the ADC cannot be biased into weak inversion, since the amplifiers inside the ADC should have a bandwidth of at least 5 times the sampling speed (assuming switch-capacitor circuits). Based on this transistor-level analysis, multiple ADCs in parallel can be more power efficient if a suitable ADC architecture can be found that is at least as effective as a typical chip-level architecture (e.g. a pipeline ADC).

When we compare column-level and pixel-level ADCs reported in literature, it is immediately obvious that pixel-level ADCs are impractical for low-cost sensors due to their large pixel sizes. Moreover, the power consumption is probably not determined anymore by required transconductance, but by a minimum bias because of leakage currents, which will decrease the power efficiency. Therefore, column-level ADCs are the best compromise between necessary speed and amount of parallel circuitry. In the next paragraph, we will briefly describe some circuit aspects of such column-level ADCs.

### 4.3 Flexible power/quality settings

Based on the assumption that a column-parallel ADC is the best topology to minimize power consumption, the next step in an ADC design for ambient

intelligence is to design the ADC in such a way that the quality it delivers can be varied in order to vary the power consumption. This can be of particular interest in systems that do not have to deliver a high quality image most of the time, for instance a motion-detection camera. When the camera image is only stationary, no high quality picture is needed, however, when motion is detected, a higher quality is desired.

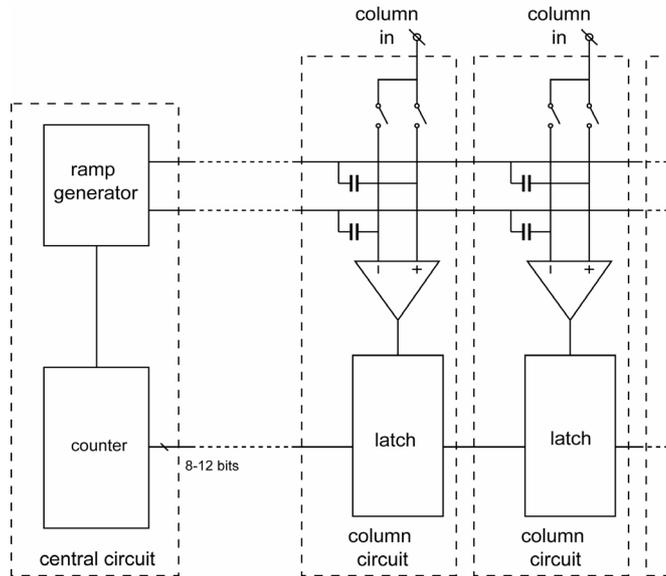


Figure 3.3-13. Column-parallel single-slope ADC architecture.

This flexible quality and power can easily be implemented into a column-parallel ADC, if a single-slope architecture is used.<sup>28,29</sup> In Figure 3.3-13, a block diagram of such architecture, which is commonly used for column-level ADCs, is depicted. It consists of a single-slope ADC system, where a single, central ramp generator is driving a large number of comparators that are situated in each column. A central digital counter runs synchronized with the ramp generator and is connected to digital latches in each column. When a comparator detects that the ramp voltage exceeds the signal, the digital latch is triggered and a digital output is stored. The advantage of this architecture is that it minimizes the amount of circuitry needed in each column. Moreover, it is relatively easy to get a uniform response across all ADC channels, as only comparator offsets can cause non-uniformities. These offsets can be corrected using the auto-zero technique.

The resolution of such an ADC depends on the steepness of the ramp and the clock speed at which the digital counter is running. Thus, the resolution

of the system can be easily changed by changing the ramp generator and/or digital counter, which are both implemented on a central level. Therefore, although the analog signal path of the ADC is column-parallel, which reduces bandwidth and noise, the ADCs quality and thereby its power, can be easily changed at one central circuit.

Since it is easiest to design the column-level comparators for one speed, it is best to design them such that they are fast enough to convert an analog signal at the highest quality at the required speed. When a lower quality is needed, the steepness of the ramp can be increased, thereby reducing the resolution. As a result, the A/D conversion time decreases, and the comparators can be powered down for some of the time, thereby reducing power consumption.

Apart from changing the ramp steepness, we can also create a companding ADC by changing the shape of the ramp. When the ramp voltage is exponential, a dynamic compression of the input signal takes place, as is done in telephony systems. This can further reduce the power consumption. In particular, we can exploit the fact that some of the noise in an imaging signal increases at high signal values, due to photon shot noise in the pixel. Therefore, the resolution of the ADC can be decreased for high input signals without losing imaging quality.

## 5. SPECIAL DESIGNS

Technological improvements in the area of CMOS VLSI have fashioned devices to be more power efficient and cheaper, thus making it a suitable candidate for AmI applications. Moreover, a circuit designer has more flavors of architectures to choose from either to meet the stringent power requirements of AmI systems or that use specialized designs to achieve unique characteristics.<sup>33</sup> Logarithmic pixel and various current mode architectures can lead to very low power consumption. In the next level of hierarchy, a part of the computation usually processed in DSPs can be shifted to the pixel themselves by various spatial arrangement of the sensors that mimic the biological systems. In addition, employing massively parallel analog processing units for low-level image processing in the pixels further reduces the computational power budget of DSPs and ASICs that follow the chain. Proper selection of the fabrication techniques to realize these sensors can also help optimize the energy budget of a system. For example, SOI (Silicon on Insulator) techniques can be implemented for very low voltage and power applications. A brief description of these various techniques that can be used to improve the power budget for AmI systems or address special needs will be presented.

## 5.1 Various electrical structures

### 5.1.1 Logarithmic structure

The logarithmic structure, which has a logarithmic response to input radiation, is a good example of a *continuous response* pixel (see Figure 3.3-14). In this pixel architecture, the reset transistor (T1) operates in weak inversion mode since only a very small current flows through the load transistor when light is incident on the photodiode.

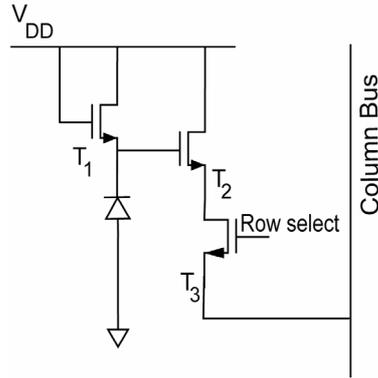


Figure 3.3-14. A logarithmic pixel structure.

The current that flows through T1 can be written as

$$I = I_0 \exp\left(-\frac{V_g - V_s - V_{th(T1)}}{nV_t}\right),$$

where  $V_s$  and  $V_g$  are the source and gate voltages and  $V_{th(T1)}$  is the threshold voltage of the load transistor.  $n$  and  $I_0$  are process dependent parameters and  $V_t$  is the thermal voltage. The output voltage can be written as

$$V_A = V_{DD} - V_t \ln\left(\frac{I_{ph}}{I_0}\right).$$

The power consumption for an array of  $525 \times 525$  pixels, employing the above structure in addition to on-chip calibration for FPN noise and ADC, can be typically some hundreds of milliwatts.<sup>34</sup> These pixels have the capability of capturing images with illumination ranges exceeding 120dB.

However, these pixel structures do suffer heavily from FPN, and image lag. Studies are being carried out to improve the noise factor and enhance the image quality.

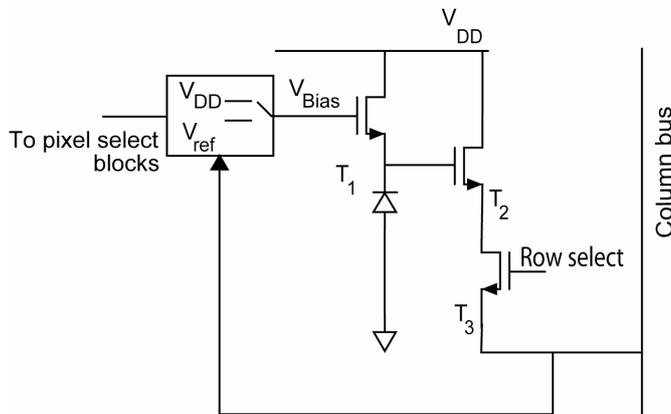


Figure 3.3-15. Lin-Log mode of pixel operation for smart systems.

AMI applications can also make use of the *Lin-Log* mode of pixel operation (see Figure 3.3-15).<sup>35</sup> Here, by choosing the value of  $V_{bias}$ , the pixel can be chosen to operate either in the linear or in the logarithmic mode of operation. Thus, the image can be first captured using the *Log* mode of operation, and by using threshold and feedback blocks, the linear mode of operation can be carried out for specific pixels or region of interest by clever pixel select logic blocks. This effectively reduces the power consumption of the system.

### 5.1.2 Current mode pixel architectures

Current mode pixel structures greatly simplify integration of on-chip signal processing and lead to increased dynamic range while maintaining faster readouts and using a smaller silicon area. They are better suited for applications involving low voltages and are inherently buffered against voltage fluctuations. Current mode pixels tend to have large FPN, and efforts are on to rectify this problem.<sup>36</sup>

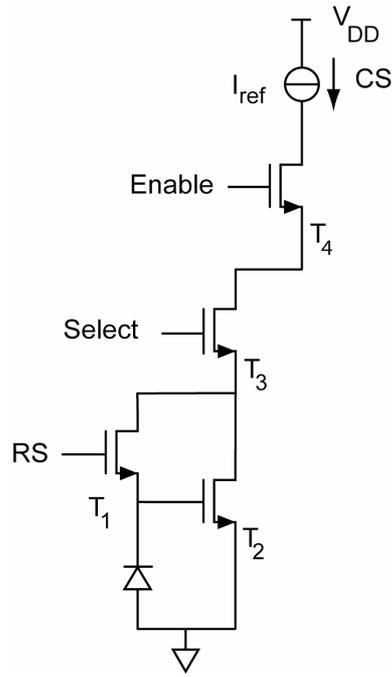


Figure 3.3-16. A current mode pixel employing a current mirror (T1 and T2).

Figure 3.3-16 presents such a configuration. During reset, transistors T1, T3, and T4 are on so that a known reference current  $I_{ref}$  given by

$$I_{ref} = \frac{1}{2} \beta (v_{gsT2} - v_{thT2})^2$$

and flows through T2 and the gate voltage of T2 is “reset” to a voltage given by

$$V_{ref} = \sqrt{\frac{2I_{ref}}{\beta}} + v_{thT2}.$$

After an integration time,  $t_{int}$ , and a given photo current,  $I_{photo}$ , the voltage at the gate of T2 is reduced to  $V_{gsT2} = V_{ref} - \Delta V$ . This voltage can be read out as a current by closing T3 to connect the pixel to the column bus.

Furthermore, readout almost independent of threshold voltage of T2 is possible by keeping T4 enabled (automatic cancellation of FPN)<sup>37</sup> thus reducing the number of processing steps later in the chain.

### 5.1.3 The silicon retina chip for Aml

There have been improvements in smart system design based on biologically inspired structures. For most Aml applications, retina-like vision systems are well suited for object tracking and identification. The fovea and periphery approach introduces a higher concentration of sensors in the fovea and an exponential decay of the density towards the periphery (log-polar imaging array). This architecture increases the data compression and lowers the power budget.<sup>38</sup> The power consumption of such a system can be made as low as 25mW at video frame rates of 28fps.

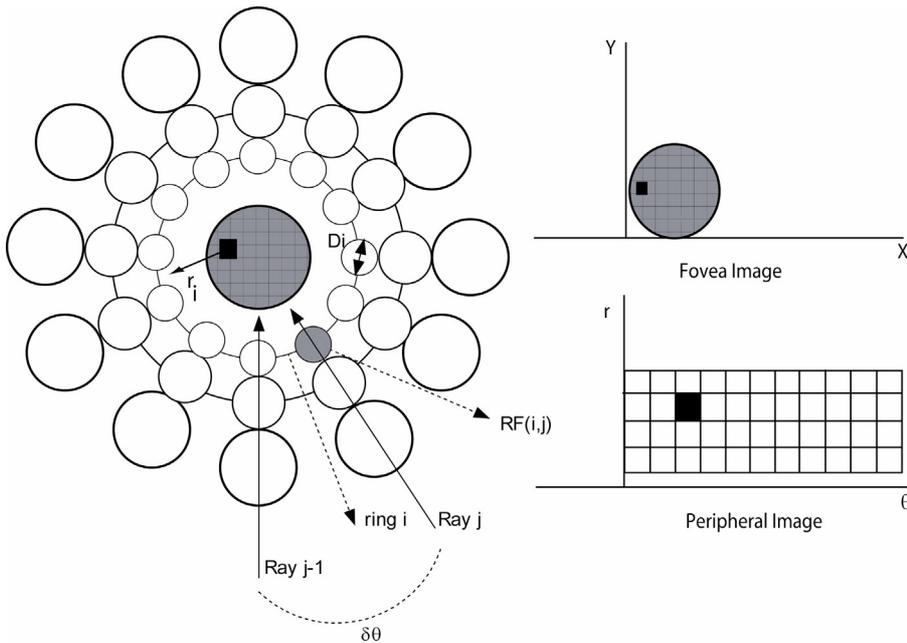


Figure 3.3-17. A foveated-mapping scheme.

Image coordinates are mapped from the original image via a mapping template (a) to separate images for the fovea and the periphery. Data in the original image undergoes a one-to-one mapping to the fovea image. In the periphery, the receptive fields (RF) or the circles in Figure 3.3-17 cover multiple pixels. Hence, the data corresponding to a RF undergoes a many-to-one mapping in which all pixels within a receptive field are averaged to produce a single pixel value in the periphery image. RF's in the periphery are distributed along rays of angular displacement,  $\Delta\theta$ . All RF's on ring  $i$

have radial displacement given by  $r_i = \alpha e^{j\beta}$  where  $\alpha$  and  $\beta$  are determined by solving the equation for the given inner and outer edges of the periphery.

#### 5.1.4 Pixel parallel analog processing

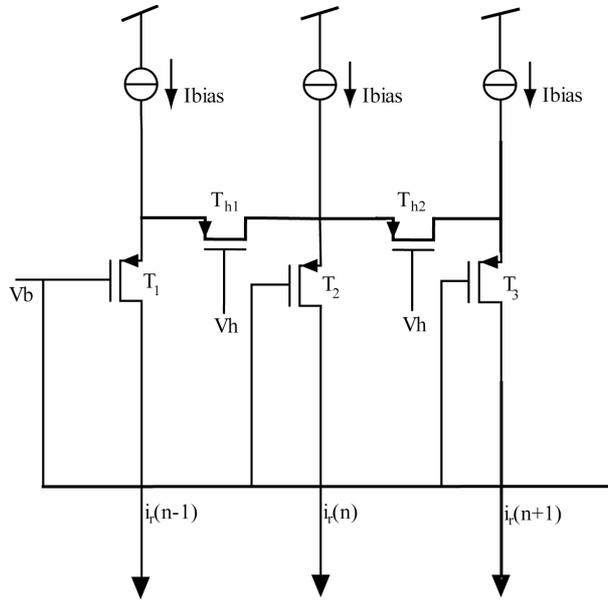


Figure 3.3-18. Weak inversion transistor network possessing a linear relationship.

Analog processing in a parallel fashion in the pixels helps to reduce the computation budget that follow the chain. These computations can be considered as filters. Such filters can be realized by analog circuits, which have complex-valued impulse responses. For example, a filter has been implemented by Shi,<sup>39</sup> which provides an orientation selective system. These filters can be electronically tuned by varying the bias voltages. One advantage of such filters is that they operate in continuous time. As an example, Figure 3.3-18 shows a section of a filter based on transistors operating in the weak inversion regime where the energy efficiency is maximized. The filter function can be thought of as the weighted sum of the pixel currents and a constant term. Transistor networks in weak inversion as shown in Figure 3.3-18 can realize such functions. The output signal, i.e., the processed image, provides a mechanism for differentiating object orientations.

In Figure 3.3-18, the weight of the coefficients of the filter function can be set by choosing the values of  $V_b$  and  $V_h$  appropriately. The value as a function of  $V_b$  and  $V_h$  is given by:

$$\alpha_w \propto e^{\frac{k}{V_T}(V_b - V_h)}$$

Current additions and subtractions can be performed at the nodes of the circuit. Current amplification, both positive and negative, can be performed by current amplifier circuits consisting of current mirrors. Thus the currents indicated by  $i(n-1)$ ,  $i(n)$ , and  $i(n+1)$  are effectively the terms comprising the filter function. A network of such systems can be utilized to realize a filter completely, once the filter transfer function is known.

The power dissipation of such pixels is reported to be around  $1.2\mu\text{W}$  per pixel.<sup>39</sup>

### 5.1.5 Pixel parallel analog to digital converters

As pixel readout is not limited by settling time as in column readout, pixel ADCs are an attractive solution for high-frame rate, low-power systems particularly for Aml applications. This also prevents the transfer of analog charges through long readout buses. A pixel parallel ADC employing the concept of a first-order synchronous  $\Sigma$ - $\Delta$  A/D converter is discussed below.<sup>25</sup>

A free-running continuous oscillator when sampled at fixed intervals can be seen as a first order  $\Sigma$ - $\Delta$  ADC. Since it is a sampled free-running oscillator, it does not require clocked components and consists only of a single comparator.

The simple representation of a time mode pixel represented in Figure 3.3-19 compares continuously the node voltage of the diode and switches state when the voltage crosses a threshold value  $V_{low}$ . This information is obtained in the column bus as a PWM signal whose width corresponds to the slope of the integration curve. Pixel structures with power dissipation of less than  $40\text{nW}$  per pixel have been reported using this approach.

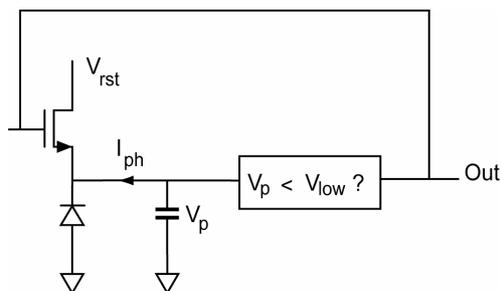


Figure 3.3-19. Time mode pixel architecture.<sup>25</sup>

## 5.2 Structures at the fabrication level

Advancements in the area of fabrication technology have also helped improve the performance of sensors.

The SOI technology offers full dielectric isolation and various quasi-ideal properties like sharp sub-threshold slope, low body effect, and high temperature operation as well as radiation hardness. These devices also promise low power operation, owing to the better coupling between the gate voltage and surface potential than in the bulk devices. The power dissipated in a circuit is proportional to  $f \times C \times V^2$  where  $f$  is the frequency of operation,  $C$  is the sum of all capacitances in the circuit, and  $V$  is the supply voltage. Since all capacitances except the oxide capacitance are less in SOI devices, they dissipate less power as well. This makes a SOI device a good candidate for AmI applications. Figure 3.3-20 shows a hybrid bulk/SOI device structure.<sup>40</sup> In this device, the photodiode was fabricated in the usual SOI technique by an extra etching step to remove the buried oxide.

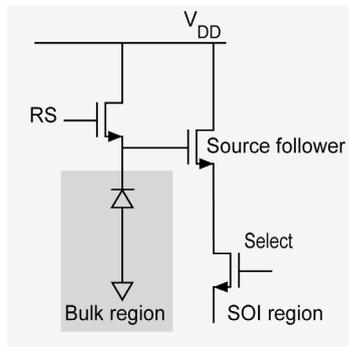


Figure 3.3-20. Layout of a hybrid bulk/SOI CMOS active pixel image sensor.

## 6. SUMMARY AND OUTLOOK

Some promising approaches that can reduce the power budget of image sensors fabricated in CMOS VLSI technology have been discussed. Options have been presented to improve and/or integrate the various structures for applications pertaining specifically to ambient intelligence. It is anticipated that new and/or improved designs will come along at an amazing rate, which, in turn, will lead to innovative uses that have not yet been contemplated. Use will be accelerated if interfacing standards are to be developed. A bright future awaits the CMOS image sensor, and chip designers will enjoy myriad challenges.

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