A CMOS Imager With Column-Level ADC Using Dynamic Column Fixed-Pattern Noise Reduction

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***Abstract*—This paper presents a CMOS imager with column-level ADC that uses a dynamic column fixed-pattern noise (FPN) reduction technique. This technique, called dynamic column switching (DCS), strongly reduces the perceptual effects of nonuniformities introduced by the column-level ADC or any other column-wise circuit element. This relaxes the uniformity requirements on the column-level ADC circuitry, which can significantly decrease power consumption and chip area. The proposed DCS technique requires only five transistors per column and minimal digital overhead at the chip level. A prototype was realized in a 0.18 μm CMOS process. The implemented column-level ADC uses a single-slope architecture and features a low-power column circuit design. In the measured images, the application of dynamic column switching make a column FPN of $\pm$0.67% of full scale nearly invisible to the human eye.**

***Index Terms*—A/D conversion, CMOS image sensors, column FPN reduction, column-level ADCs, dynamic offset cancellation.**

I. Introduction

In RECENT years, rapid research and development have helped make CMOS imagers a mature alternative for the more conventional CCDs [1]. This development has been fuelled by mobile consumer applications, in particular cell phones. For these battery-powered, portable devices, CMOS imagers are very well suited. First of all, their power consumption tends to be about a factor of three lower than CCDs. Moreover, the signal-processing circuitry can be co-integrated on the same die as the image sensor, resulting in a camera-on-a-chip. This enables the creation of miniature, low-cost single-chip camera modules that can directly be interfaced with a microprocessor or a cell phone baseband chip.

While the first of such camera modules typically offered a CIF (352×288 pixels) or VGA (640×480 pixels) resolution [2], there is currently a strong push in the industry to increase the pixel count of the imager, leading to low-cost CMOS imagers with several millions of pixels [4]. It is doubtful whether such high pixel counts lead to an actual increase in resolution, i.e. an increased ability of the imager to resolve spatial variations in light intensity. In most cases, the quality of the optics used will be the limiting factor. Nonetheless, the increase in pixel count has profound implications on the imager design. Firstly, the pixel size has to be decreased in order to increase the pixel count, since increasing the die area is not attractive because of higher costs and a bigger camera module. Secondly, since more pixels have to be read out, the interface electronics of the imager need to have a higher speed. This requires changes at the architectural level, particularly for the on-chip analog-to-digital conversion.

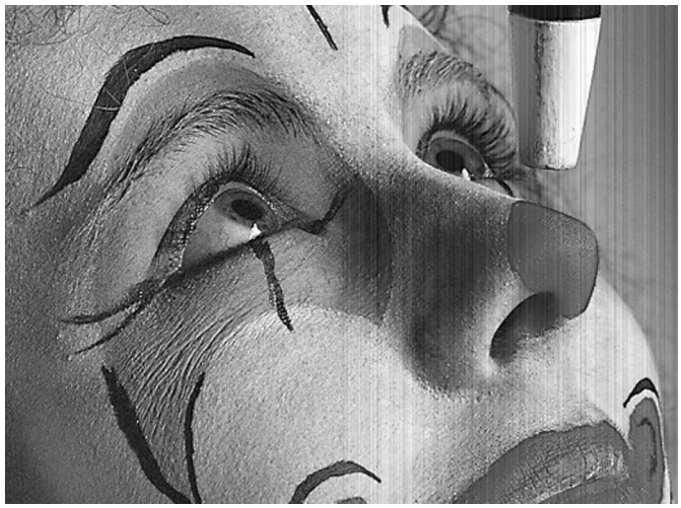

Fig. 1. Simulation comparing pixel and column FPN. In the left half of the image, 3% pixel FPN is added, in the right half 3% column FPN.

Early commercial CMOS imager modules were usually equipped with a single, chip-level ADC [2], [3]. However, as pixel count continues to increase, it has become increasingly difficult to use such an approach, as it requires an ADC with a speed of several hundreds of Msamples/s. An alternative approach is a column-level ADC, where hundreds or even thousands of ADC channels are operating in parallel. As a result, each channel can operate at a much lower speed and at a very low power. The main drawback of this approach is that any mismatch between the ADC channels leads to column fixed-pattern noise (FPN), which can severely degrade the perceived image quality. Column FPN can be observed as vertical stripes in an image that are visible even if the magnitude of the column FPN is much lower than the pixel FPN and/or temporal noise present in an image, such as white noise and photon shot noise. Previous work [5]–[8] has shown that it is possible to realize a column-level ADC with sufficient column-to-column uniformity as to not produce any visible artefacts. However, the uniformity requirement puts a severe design constraint on the column circuit, which can lead to higher power consumption

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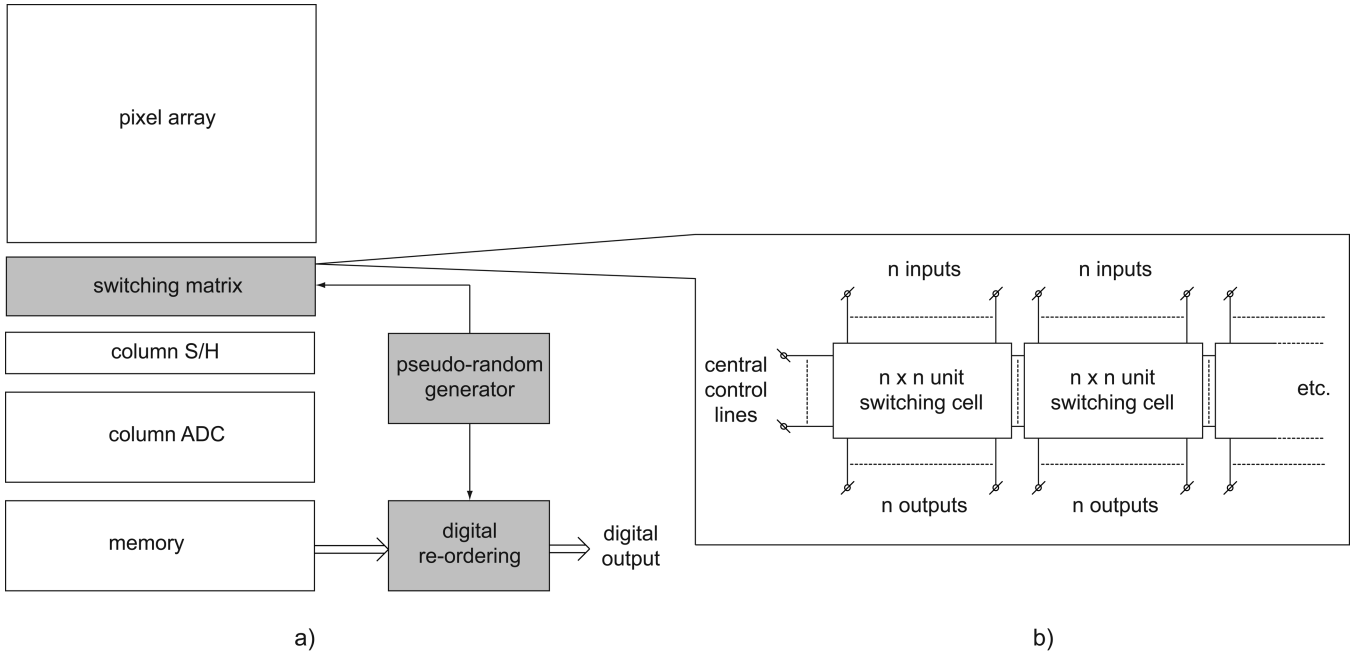

Fig. 2. (a) Block diagram of the sensor. The gray blocks were added to implement DCS. (b) partitioning of the switching matrix block into unit switching cells.

and more chip area, as well as a lower yield. The reduction technique proposed in this paper, called dynamic column switching (DCS) relaxes the column circuit design requirements, thereby potentially reducing power consumption and chip area.

This paper is organized as follows. In Section II, the principle of DCS is described. Section III presents simulation results. Section IV discusses the details of the implementation. Experimental results are presented in Section V. Finally, conclusions are presented in Section VI.

II. Dynamic Column Switching Principle

The main problem of column FPN in an image is not its actual magnitude, but its perceptual effect observed by the human visual system, as is illustrated in Fig. 1. In this synthetic image, a Gaussian pixel FPN with a standard deviation of 3% of full-scale has been added to the left half of the image, while column FPN with the same magnitude was added to the right half of the image. It is obvious that the column FPN is much more visible than pixel FPN, because of its spatial correlation, i.e. every column has a systematic error caused by offset and gain variation of the associated column ADC channel. Although it is hard to quantify this perceptual difference between pixel and column FPN, it has been proposed [9] that random column FPN is five times more harmful to the perceived image quality than pixel FPN. Therefore, since pixel FPN is typically around 0.5%, a column FPN of about 0.1% or less is necessary to get a sufficiently high perceived image quality.

While existing column-level ADC designs have so far relied exclusively on reducing the magnitude of column ADC nonuniformities, the dynamic column switching technique described here reduces the perceptual effect of these nonuniformities. This is done as follows: a switching matrix is placed between the column buses of the pixel array and the rest of the column circuitry, as illustrated in Fig. 2(a). At the beginning of each line time, the state of the switching matrix is changed before the pixel array is read out. As a result of this dynamic column switching (DCS), each column ADC channel is used to read out not just one, but several columns of the imaging array, thus spreading the nonuniformity of the column circuit over several array columns. Since the switching matrix changes the order in which the pixel outputs are sampled, some extra circuitry is necessary to restore the original pixel output order. This can be easily done on-chip in the digital domain.

A crucial part of the design is the switching matrix between the imaging array and the column ADC. It is obvious that it is impractical to design a switching matrix that can connect *any* column of the imaging array to *any* ADC channel, as this would require a very complex set of switches and wires. Therefore, our approach is to divide up the array into smaller unit switching cells that can connect just n columns of the imaging array to n column ADC channels, all of them controlled by the same control lines Fig. 2(b). The choice of n is a design trade-off: a larger switching cell leads to a better spread of the nonuniformities of the column ADC channels, at the expense of a higher switching cell complexity, which means more chip area. Since it is difficult to predict the perceptual effect of DCS analytically, the choice of n is mainly based on simulation results. Such simulations will be described in Section III.

Finally, it should be noted that the proposed technique has some obvious limitations. First, since the magnitude of the column ADC nonuniformities is not reduced, applying DCS effectively increases the pixel FPN, as column uniformities are transformed into pixel (-like) nonuniformities. This means that the initial column nonuniformities should be smaller then the expected pixel FPN. Second of all, the required division of the switching array into small unit switching cells renders the technique ineffective for nonuniformities that are strongly correlated between adjacent columns. For instance, DCS would

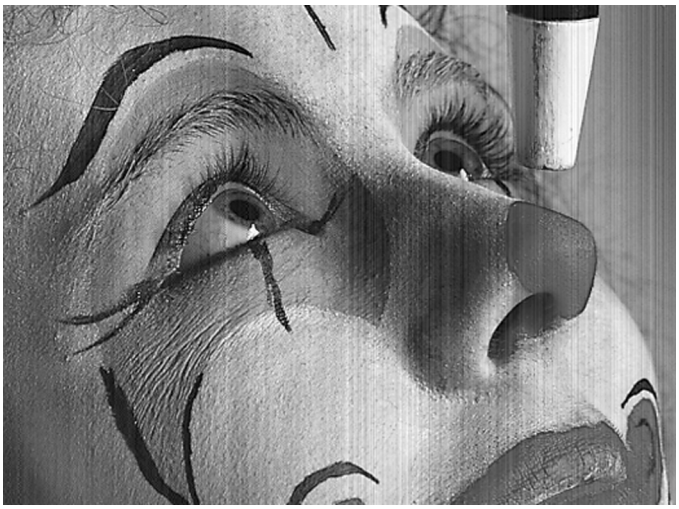

Fig. 3. Simulation of DCS on a sample image to which 3% column FPN is added, using a 2×2 unit switching cell.

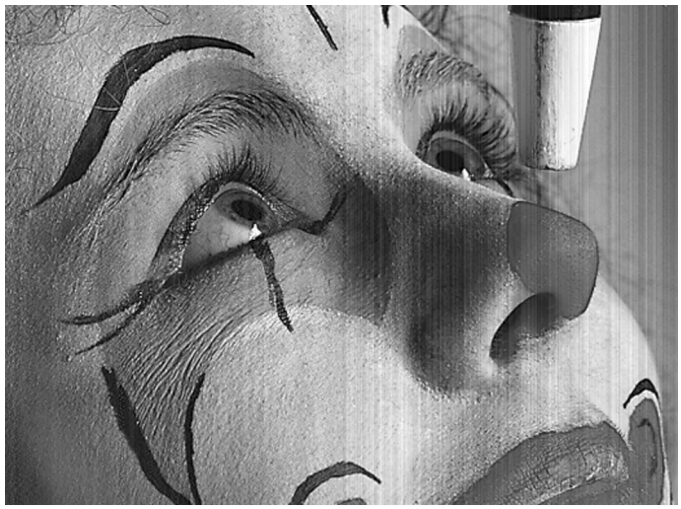

Fig. 5. Simulation of DCS on a sample image to which 3% column FPN is added, using a 4×4 unit switching cell.

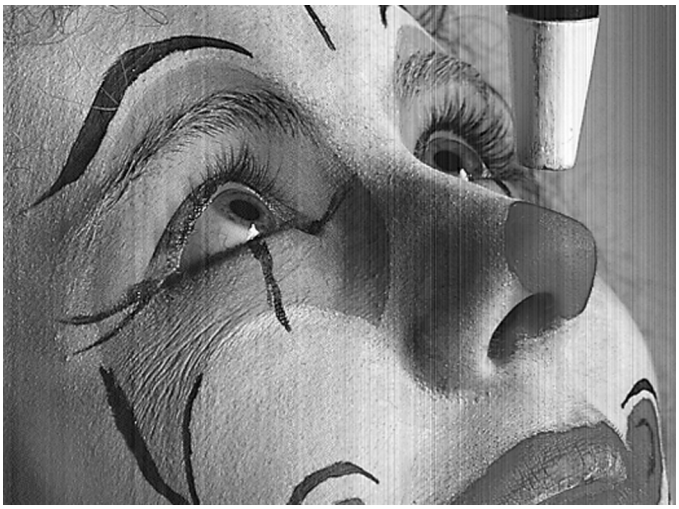

Fig. 4. Simulation of DCS on a sample image to which 3% column FPN is added, using a 3×3 unit switching cell.

Fig. 6. Simulation of DCS on a sample image to which 3% column FPN is added, using a 5×5 unit switching cell.

not be effective against an offset gradient that goes from one side of the column to the other. However, in a proper column ADC design, the main source of nonuniformities is process spread, which can usually be considered to have a Gaussian distribution. In such cases, the column FPN can be expected to decrease by a factor equal to the square root of n, where n is the number of columns being switched, since it is essentially Gaussian noise that is averaged. However, such a mathematical analysis does not account for the perceptual effects of DCS. In the next section, such perceptual effects will be studied using simulations.

III. Simulation Results

As discussed in the previous section, the complexity of the switching matrix is the main design variable in applying DCS. This switching matrix should be divided into unit switching cells that connect n imaging array columns to n column ADCs, where a larger n is expected to yield better results at the cost of a higher switching cell complexity. Using Matlab simulations, the perceptual effects of DCS for different values of n were evaluated. Results of such simulations are depicted in Fig. 3–6. In all figures, a Gaussian distributed column FPN of 3% of full scale was added throughout the sample image. While this is far too much column FPN to yield an acceptable image quality, also with DCS, it is very well suited for comparative purposes, as all effects become more visible. In every image shown, DCS was applied only to the left half of the image, enabling a direct comparison within one image.

In Fig. 3, the visual effects are shown for the simplest switching matrix, with $n = 2$, which was already shown in [10]. Although such a switching matrix does decrease column FPN, it remains quite visible in the left half of the image, as only two adjacent columns are alternated to spread the column FPN. Much better results can be obtained with more complex switching cells that switch $n = 3$ through five inputs to outputs, as depicted in Fig. 4–6. As expected, DCS is more effective for more complex switching schemes, although the increase in

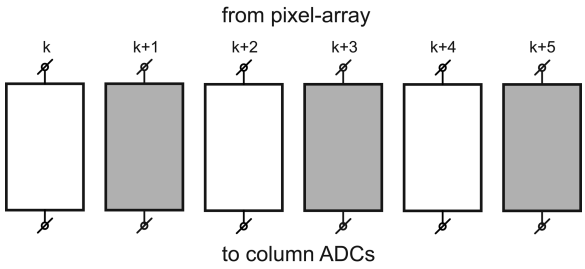

Fig. 7. Block diagram illustrating the interleaving of two 3×3 unit switching cells to increase the spatial spreading of column FPN.

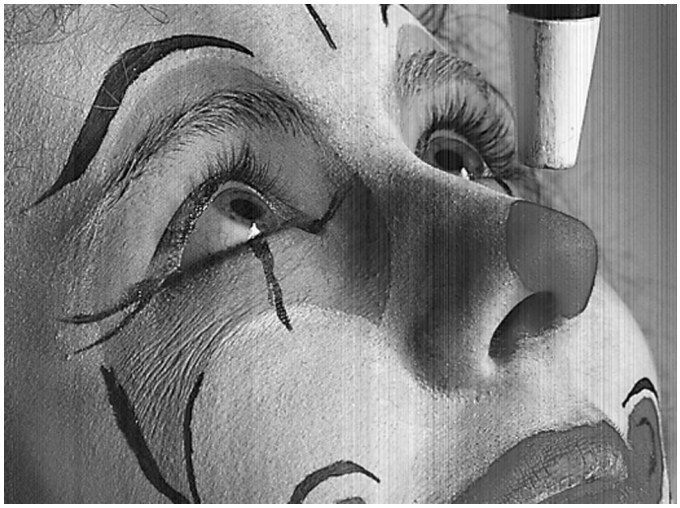

Fig. 8. Simulation of DCS on a sample image to which 3% column FPN is added, using two interleaved 3×3 switching cells as unit for the switching matrix.

effectiveness becomes progressively less for higher n. This corresponds well with the Gaussian noise model, which predicts that the decrease in column FPN should be proportional to the square root of n.

Even for $n = 3$, the simulation results show very acceptable results given the very high initial column FPN, with the exception of some wider residual stripes that are visible. The explanation for such stripes is as follows: since the column FPN is only spread over three columns, the chosen set of columns may sometimes have an average offset that differs significant from the overall average of the image. While it is possible to decrease this residual effect by increasing n, this is unattractive as the complexity of the switching matrix rapidly increases. Instead, an alternative solution was found. Two switching cells of $n = 3$ are interleaved with one another, i.e. one circuit is connected to column k, $k + 2$ and $k + 4$ while the second is connected to column $k + 1$, $k + 3$, and $k + 5$, as depicted in Fig. 7. This results in more spatial spreading of residuals, since any three columns that are averaged by a unit switching cell are not adjacent to one another, but are interleaved with another set of three columns. This reduces the visibility of any residual column FPN, as shown in Fig. 8. Here again, 3% column FPN is added throughout the image, while DCS is applied in the left half of the image using 3×3 unit switching cells that are interleaved.

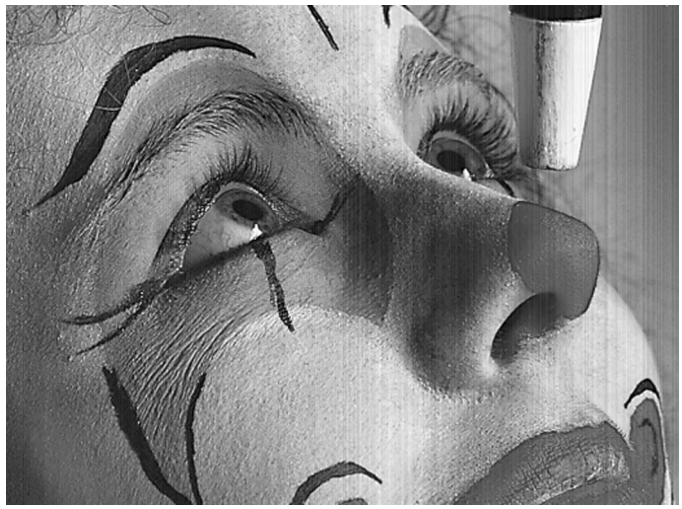

Fig. 9. Simulation of DCS on a sample image to which 2% column FPN is added, using two interleaved 3×3 switching cells as unit for the switching matrix.

Fig. 10. Simulated effect of DCS on a sample image to which 1% column FPN is added, using two interleaved 3×3 switching cells as unit for the switching matrix.

To further evaluate the perceptual effects for a lower amount of column FPN, simulations using the same interleaved 3×3 switching cell were performed for 2% and 1% column FPN, as depicted in Figs. 9 and 10. As can be seen from the figures, residual column FPN is hardly visible for an initial column FPN of 2%, while a column FPN of 1% is rendered invisible using DCS. Therefore, a unit switch consisting of two interleaved 3×3 switching cells was selected to be implemented in a prototype CMOS imager, which will be described in detail in the next section.

IV. Implementation

A. Sensor Overview

To test the dynamic column switching technique, a prototype imager was implemented in a standard single-poly four-

TABLE I
SPECIFICATIONS OF THE PROTOTYPE

Technology	1P4M 0.18μm CMOS
Die Size	5.4mm x 4.5mm
Supply Voltage	2.8V/1.8V
Pixel Pitch	5.6μm
Pixel Type	3T
Fill Factor	47%
Number of Pixels (on layout)	680 x 512
Number of Pixels (read out)	340 x 512
ADC architecture	Single-slope
Column ADC Pitch	11.2 μm
ADC resolution	10b
ADC read-out noise	150μV
ADC LSB voltage	600μV

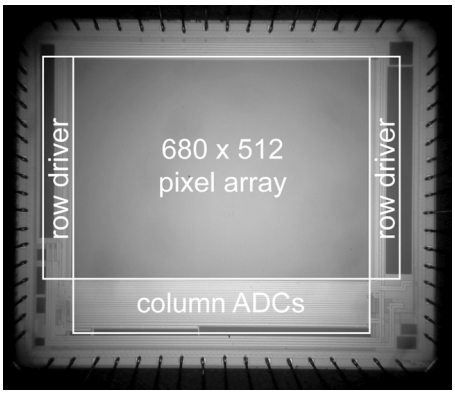

Fig. 11. Chip micrograph of the prototype imager.

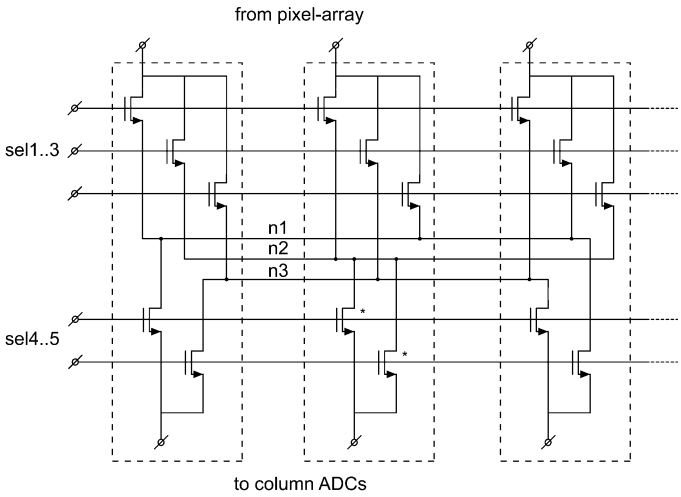

Fig. 12. 3×3 switching matrix element.

metal 0.18 μm CMOS process. The prototype has a resolution of 680×512 pixels and has a pixel pitch of 5.6 μm. For the prototype, standard 3T pixels with nwell photodiodes were used. The chip size is 5.4 mm×4.5 mm. The column ADC uses the well-known single-slope architecture, as shown in [6]–[8]. To facilitate the layout of the column ADC, the column pitch was designed to be twice the pixel pitch (11.2 μm). In order to read out the pixel array, it was intended to place column ADCs both above and below the imaging array. Unfortunately, practical restrictions on this prototype prevented the placement of column ADCs above the imaging array, which reduced the amount of pixels that can be read out to 340×512 pixels. The prototype uses a 1.8 V supply voltage for the analog circuitry and a 2.8 V supply for the pixel, digital and I/O circuitry. Fig. 11 shows a chip micrograph of the imager, and Table I summarizes the prototype specifications.

B. Dynamic Column Switching Circuitry

To reduce the column FPN using the DCS technique described in the last two sections, a unit switching cell with three inputs and three outputs is required. As indicated in Fig. 2, these switching cells are inserted into the front-end of the column circuit, before the sample-and-hold capacitors. By doing so, all nonuniformities behind the switches are reduced by DCS. Moreover, the switching cells effectively become part of the sample-and-hold switches. As a result, any mismatch in their on-resistance should not cause any artefacts, provided that there is enough time for the in-pixel source follower to settle. This requirement can easily be met without large bias currents or large switches.

In Fig. 12, the unit switching cell that was used in the prototype is depicted. Since the switching cell has three inputs and outputs, there are six distinct ways to connect the inputs to the outputs. In each column, five transistors are required for the switch, and their gates are connected to control lines that are identical for all unit switching cells in the column. Three transistors are used to connect the column bus to one of the three intermediate nodes ($n1$, $n2$, $n3$). This is done by control lines $sel1$ through $sel3$, of which only one is enabled at any time. Thus, there are three different ways of connecting the inputs to the intermediate nodes. Furthermore, each column contains another two transistors that connect the intermediate nodes ($n1$, $n2$, $n3$) to the switch outputs, by means of control lines $sel4$ and $sel5$. Again, only one of these control lines is enabled at any time. Thus, there are two different ways of connecting the intermediates node to the outputs, and as a result there are six different ways of connecting inputs to outputs. As can be seen in Fig. 12, the middle column contains two transistors marked with an asterisk $(*)$ that do not have an actual switching function, but are rather used as dummy switches to maintain layout uniformity. To ensure an acceptable on-resistance of the switches for all signal levels, control line voltages of 3.3 V are used

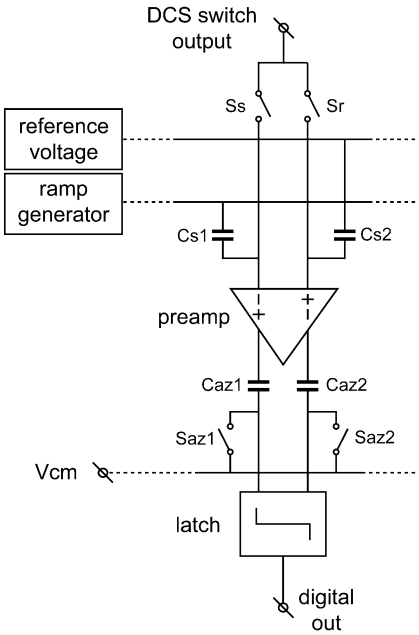

Fig. 13. Overview of the analog column circuitry.

in combination with 3.3 V capable transistors with a W/L of 1.2 μm/0.6 μm.

As described in Section III, two 3×3 unit switching cells are interleaved with one another, as illustrated in Fig. 7. Using the unit switching cell described above, this can be easily accomplished by adding a second set of three intermediate nodes in each column. This second set of nodes interconnects the unit switching cell connected to columns $n+1$, $n+3$, and $n+5$, while the first set of nodes interconnects the unit switching cell connected to columns n, $n+2$, and $n+4$.

The switch select lines $sel1$ through $sel5$ are controlled by a digital pseudo-random number generator that changes the state of the switches at the beginning of every line time. To prevent charge injection from the DCS switching matrix from degrading the imaging signals, this state change is performed before the pixels are connected to the column. For the prototype, the pseudo-random number generator was implemented as a 10 bit maximum-length linear-feedback shift register on an off-chip FPGA for flexibility. The same FPGA was used to restore the order of the digital output.

C. Column Comparator Design

In a column-parallel single-slope ADC, the column comparator tends to consume most of the power, and determines the overall ADC performance to a large extent. Therefore, the main focus during the column comparator design was to reduce its power consumption as much as possible. Fig. 13 gives an overview of the analog column circuitry [11]. The input sampling capacitors $Cs1$ and $Cs2$ are connected in a manner similarly to [8]. One side of the capacitors is connected to the column bus via switches Sr and Ss, while the other side is connected to the ramp generator and a reference voltage. When the pixel output is sampled, the ramp generator output equals the reference voltage, and therefore the voltage difference that is sampled on capacitors $Cs1$ and $Cs2$ equals the signal minus reset voltage of the pixel. After sampling, the ramp generator is activated, which effectively introduces a differential voltage onto the sampling capacitors that will compensate for the voltage difference across the capacitors. The comparator will indicate when the ramp voltage equals the differential input voltage, and the corresponding digital number is stored in a memory.

For the comparator itself, the approach was to use the minimum amount of circuitry possible for the essential comparison function, without considering secondary requirements such as offset compensation. A regenerative latch stage was used to provide most of the required gain, as such circuits offer the best gain to power ratio. However, regenerative latches usually inject charge back into their input (the so-called "kick-back effect"). If this charge were injected into an input node common to all ADC channels, it would cause large cross-talk effects. Therefore, a linear gain stage with a gain of about 30× is inserted in front of the latch.

Because of this minimalist approach, it is not possible to fully correct for offset on the circuit level, since it is difficult to perform a circuit auto-zero on a regenerative latch. Some digital offset correction is therefore necessary, i.e. a second A/D conversion with a zero input signal will be performed to measure input offset, and the result of this A/D conversion will be subtracted from the signal in the digital domain. However, if there was no circuit-level offset compensation at all, such a second A/D conversion would take a long time as the input referred offset would be large. Therefore, a circuit auto-zero is performed using capacitors $Caz1$ and $Caz2$ and switches $Saz1$ and $Saz2$ to cancel the offset of the first stage. The input referred offset of the regenerative latch is much smaller than this offset, and therefore, the required digital offset cancellation does not take a long time. As a result, the comparator uses a hybrid offset cancellation scheme: some of the offset is removed using circuit auto-zero, and some with a system-level auto-zero. A drawback of such an approach is that there will be a residual offset of ±1LSB in the output signal due to the effects of quantization noise of the offset sample. This residual offset, which could still be visible under low light conditions, was the original motivation for applying DCS to reduce column FPN.

The preamp circuit [Fig. 14(a)] has only seven transistors: a tail current source (transistor M1), a differential input pair (M2–M3), current source loads (M4–M5) and a common mode-control with transistors M6–M7 that operate in triode region. The latter transistors are replicated in the central biasing circuit [Fig. 14(b)]; as a result, the gate voltage of the replicated transistors (M11–M12) determines the common-mode output voltage of the preamp. In Fig. 15, the regenerative latch circuit is depicted [12]. As can be seen from the figure, it actually consists of two stages. The first stage, formed by transistors M1–M7, is fed by the analog power supply. To prevent large current spikes on the supply lines, a tail current source is used to limit the current consumption of the stage. As a result, the slew rate of the output voltage of the first stage is limited due to the low biasing current (1.1 μA). To overcome this speed limitation, a second latching stage is added that is not current limited and powered by the digital supply. Since this latch is not reset by the clock signal, it will only produce a power supply spike when

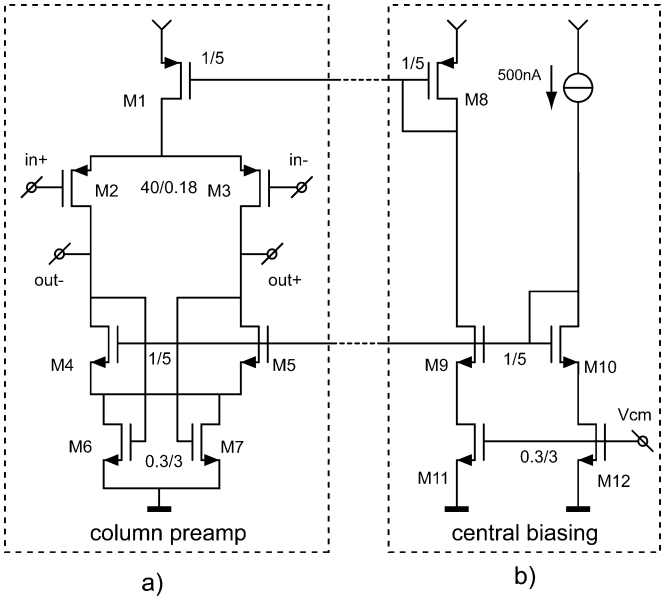

Fig. 14. (a) Circuit diagram of the preamp gain stage of the comparator. (b) Centrally implemented bias circuit for the preamp stage.

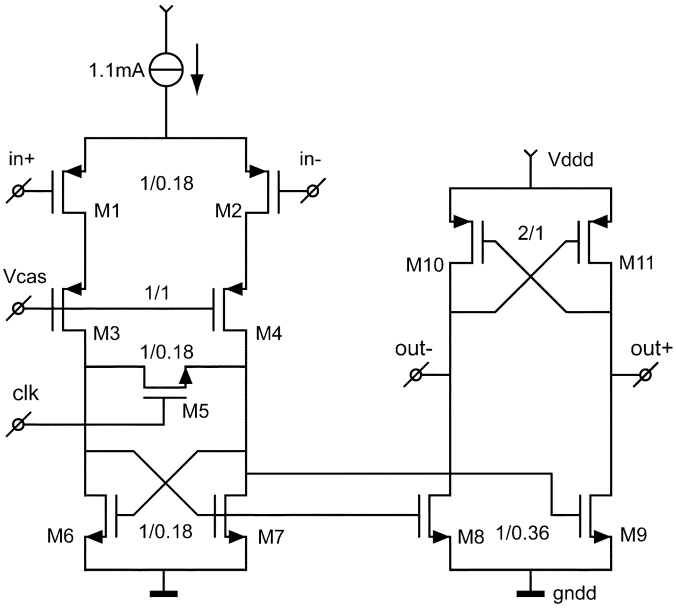

Fig. 15. Circuit diagram of the regenerative latch used in the comparator.

the output changes value. The first and second stages are interconnected with transistors M6–M9 that effectively mirror currents from the first to the second stage. All transistors in the regenerative latch are near minimum size to reduce power consumption. The resulting comparator circuit was designed for a resolution of 12 bits, which is equivalent to an LSB voltage of 150 μV. The regenerative latch can operate at a maximum clock speed of 20 MHz, and the total comparator power consumption is 3.2 μW.

V. Measurement Results

As mentioned in the last section, the ramp generator and some digital hardware were not implemented on-chip to increase flexibility in the testing phase. Therefore, the measurement

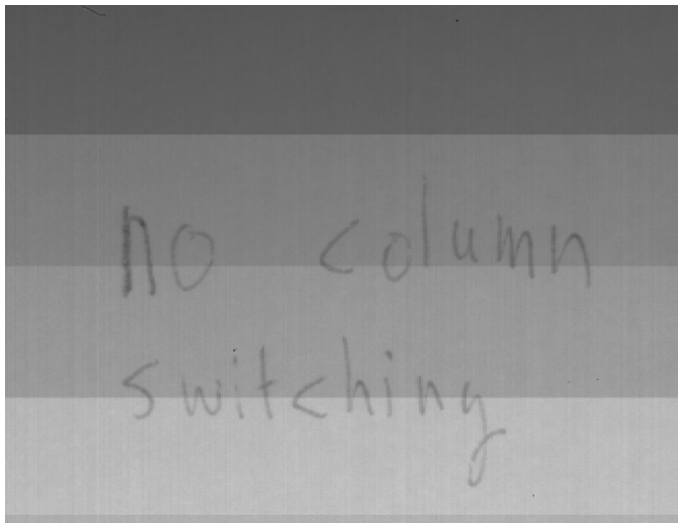

Fig. 16. Raw image captured without using DCS.

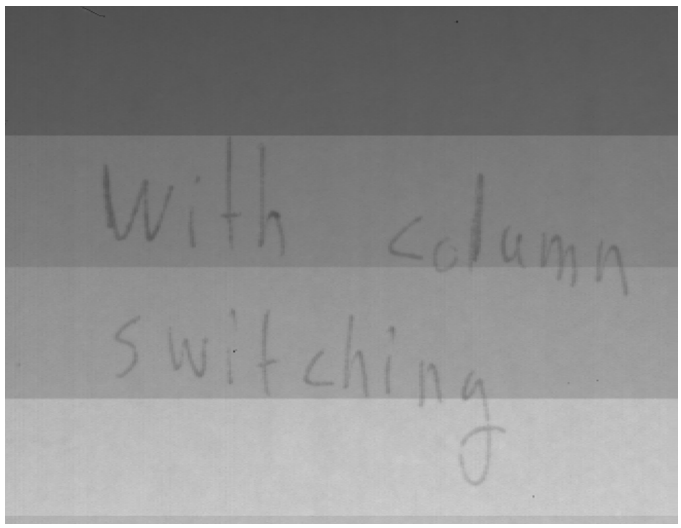

Fig. 17. Raw image captured while using DCS.

setup included an FPGA for the required digital control circuits and a high-speed DAC that was used as a ramp generator. First, the performance of the column ADC was measured via a separate test input. Measurement results showed a read-out noise of 150 μV, which limits the ADC resolution to about 10 bits. The reason for this performance decrease was found to be the noise performance of the regenerative latch, which was not properly taken into consideration during the design phase. Apart from this performance limitation, the prototype used 3T pixels, leading to a large amount of reset noise in the imaging signal. Therefore, 20 frames were averaged for all measurements on column FPN reduction to sufficiently reduce readout noise.

Fig. 16 shows a raw captured image acquired without using DCS. To make column FPN as conspicuous as possible, an image of a white piece of paper was captured (apart from the hand-written text). Furthermore, both the circuit and system-level auto-zero are intentionally switched off. As a result, the column FPN will be too high to yield an acceptable

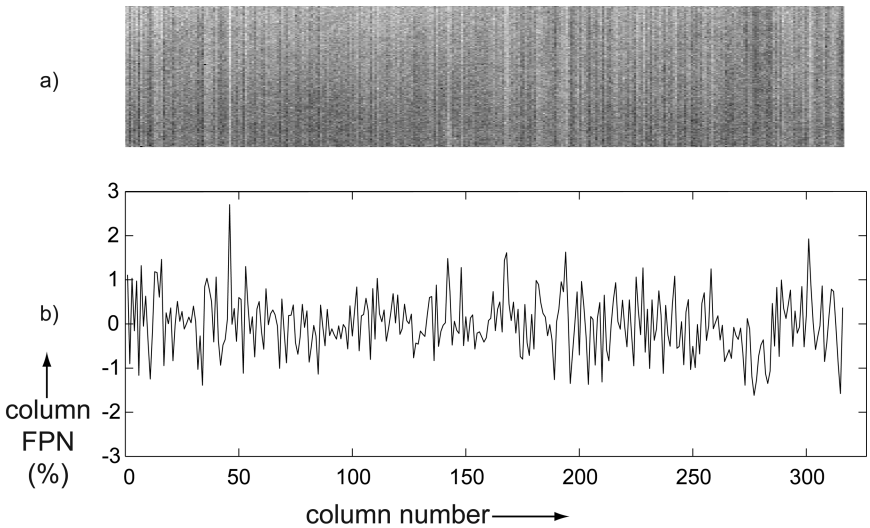

Fig. 18. (a) Contrast enhanced image region without DCS. (b) average column output, showing a column FPN of 0.67% (std. dev.).

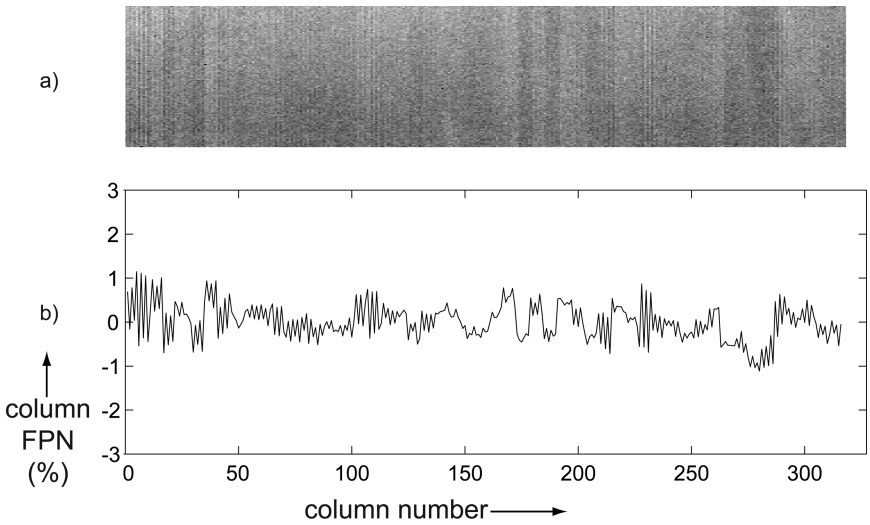

Fig. 19. (a) Contrast enhanced image region with DCS. (b) average column output, showing a column FPN of 0.41% (std. dev.).

image quality, also when applying DCS, but it makes the perceptual effect of the technique well visible. Apart from this, four horizontal bands are clearly visible in the image. This is caused by the fact that different pixel layouts were used in the imaging array, for reasons outside the scope of this paper. Fig. 17 depicts an image taken using the same parameters, but this time with DCS. It clearly shows that dynamic column switching strongly reduces the visibility of column FPN, making it nearly invisible in this image.

In order to quantify the observed column FPN reduction, the output of several rows (with the same pixel layout) was measured in uniform light input, as depicted in Figs. 18(a) and 19(a). To increase the visibility of the column FPN, the contrast in both images is enhanced 15 times. This contrast enhancement does reveal some residual column FPN in Fig. 19(a). Using these images, graphs of the averaged column outputs were made [Figs. 18(b) and 19(b)]. The average initial column FPN is $\pm 0.67\%$ (standard deviation); by using the proposed column FPN reduction technique, this is reduced to $\pm 0.41\%$. The initial peak FPN is 2.7%, and this is reduced to 1.1%.

VI. Conclusion

A CMOS imager with column ADC was presented that uses a dynamic technique to reduce column fixed-pattern noise (FPN). By switching the column ADCs between different columns of the imaging array, the perceptual effects of column FPN are strongly reduced. The prototype imager was implemented in a standard one-poly four-metal 0.18 μm CMOS process. The proposed column FPN reduction technique requires only five switching transistors per column in the prototype and a minimal amount of overhead in the digital domain. Furthermore, the presented CMOS imager features an aggressive low-power column ADC design, using comparators only consuming 3.2 μW. In the measured images, an initial column FPN of 0.69% of full scale is made nearly invisible using the proposed dynamic column switching (DCS) technique.

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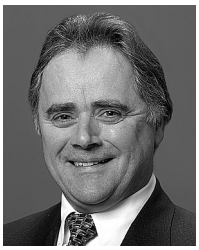

Albert J. P. Theuwissen (F'02) was born in Maaseik, Belgium, on December 20, 1954. He received the degree in electrical engineering from the Catholic University of Leuven, Belgium, in 1977, and the Ph.D. degree in electrical engineering in 1983. His Ph.D. dissertation was on the implementation of transparent conductive layers as gate material in the CCD technology.

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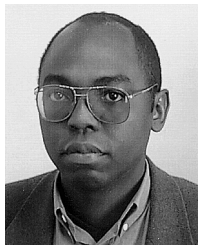

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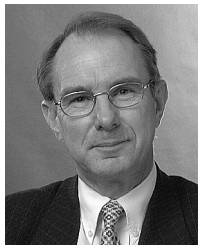

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