2.10 A CMOS Image Sensor with a Buried-Channel Source Follower

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This paper presents a CMOS image sensor with a pinned-photodiode 4T active-pixel design (APS) that uses a buried-channel source follower (BSF) as the in-pixel amplifier. A prototype of the image sensor has been fabricated in a 0.18μm CMOS process. Measurements show that compared to a regular imager with a standard nMOS transistor surface-mode source follower (SSF), the new pixel structure reduces dark random noise by more than 50% and improves output swing by almost 100%. Moreover, the new pixel structure is able to minimize the random telegraph signal (RTS) noise.

Nowadays, the random noise level of the pinned photodiode 4T APS has dropped to less than $5e^-_{rms}$, of which the major contributors are believed to be 1/*f* and RTS noise from the in-pixel source follower [1]. It is commonly accepted that the 1/*f* noise is caused by lattice defects at the Si-SiO_2 interface of the MOS transistor. As processes scale down, the RTS noise appears in pixels that have only one active interface defect. Since the exact mechanism of the RTS noise is still unknown [2] and the use of correlated double-sampling (CDS) does not fully eliminate 1/*f* and RTS noise [3, 4], no adequate technique is yet known for reducing 1/*f* and RTS noise. Therefore, these noise sources limit the imaging quality under low-light conditions. In this work, an in-pixel source follower based on a buried channel nMOS transistor is introduced, which is able to reduce 1/*f* and RTS noise. The buried channel requires an extra implantation, which pushes the highest potential in the channel away from the Si-SiO_2 interface, thus minimizing the possibility of carriers being trapped by lattice defects. As a result, the imager's read noise level can be significantly reduced. Furthermore, because the buried channel transistor has a negative threshold voltage, the pixel's output swing can be significantly improved. This means that "digital" transistors with reduced power supply voltages can be used in the pixel without limiting the pixel's output swing, saturation level and dynamic range.

Figure 2.10.1 shows the pixel circuit, the readout timing and the cross section of the BSF. Similar to a standard pinned photodiode 4T structure, the pixel consists of a pinned photodiode (PPD), a reset transistor (RST), a transfer transistor (TG), a row select switch (RS) and a source follower (BSF). A standard CDS operation is applied to cancel the threshold mismatch and reset noise. During source follower operation, the maximum potential underneath the gate is determined by the channel doping profile, the floating diffusion (FD) voltage and the column bias current. The short-dashed line in the cross section presents the channel's maximum potential. The long-dashed line presents the boundary of the depletion region.

Figure 2.10.2 shows the comparison of the simulated and measured gate characteristic of the buried and surface channel source follower transistors. Increasing the implantation dose will shift the transistor threshold voltage towards negative values, and increasing implantation energy will slightly increase the channel depth, but at the expense of higher leakage current. With the same current as used in the test pixel (6μA), the measured transconductance of the buried channel transistor is only half that of the surface-mode transistor, which leads to a longer settling time. No conclusive result on pixel random noise can be drawn from 1/*f* noise measurements on single transistors because of the noise sample-to-sample spread and the absence of the CDS filtering.

Figure 2.10.3 shows a DC measurement result of test pixels (without select transistor) to verify the threshold voltage shift and the improvement of the pixel output swing. The FD voltage is regulated through the RST signal. TG is grounded in the experiment. As shown, the maximum output swing of the BSF pixel is about 2V, nearly double that of the SSF pixels. The voltage gain of the source follower also increases from 0.83 to 0.92. From our simulation, it is shown that the lower the SF gate voltage is compared to the transistor surface potential, the higher the "potential distance" is between the channel and the Si-SiO_2 interface. Thus, it can be predicted that the channel is buried deeper for the BSF with a higher dose, and for the same BSF, reducing the bias current will help to bury the channel deeper. Because of the back-gate effect, the channel is buried deeper as the gate voltage is lowered.

Figure 2.10.4 depicts a histogram of a dark random noise measurement. The random noise of each pixel is obtained by calculating the standard deviation over 20 frames' outputs. The asymmetric distribution of the pixels around the peak of the SSF's pixel curve indicates the dominance of the 1/*f* and RTS noise of the SSF [5]. As shown, the average dark random noise of the BSF pixels is reduced by more than 50% and the noise histogram of the BSF pixels closely approximates a true Gaussian distribution with significantly reduced noise spread. Moreover, in a 120×300 BSF pixel array, no hot pixel (high 1/*f* noise) or blinking pixel (RTS pixel) has been found. In Fig. 2.10.5, the average dark random noise is plotted versus the BSF's gate bias, i.e. the FD voltage. The observed dependency confirms the relationship between pixel random noise and source follower channel depth. As noted in connection with Fig. 2.10.3, the channel is buried deeper by lower FD voltages; therefore, the measured random noise is smaller for lower FD voltages. However, a low FD voltage may introduce image lag because of the incomplete charge transfer.

Figure 2.10.6 shows a test image measured in the dark with an analog sensor gain of 10, at 30fps and with a 12b board-level ADC. The CDS interval is 1.5μs and the charge transfer period is 1μs. The upper part of the figure shows the raw data, while the lower part shows the data after a digital column-fixed-pattern noise (FPN) cancellation. The conversion gain is 73μV/e⁻. The saturation voltage is 250mV, which is due to a low fill-factor allowing several transistor configurations. The average noise is $500\mu V_{rms}$ for the SSF pixels and about $250\mu V_{rms}$ for the BSF pixels. About 0.5% of the pixels in the SSF array were observed to be RTS pixels, compared to none in the BSF array.

Figure 2.10.7 shows a chip micrograph. The pixel pitches used in the test chip are 6μm, 7.4μm and 10μm. All pixels were pinned-photodiode 4T structures and both BSF and SSF pixel types were realized in the same sensor. The prototype was fabricated in a 0.18μm 1P3M CMOS process.

A CMOS image sensor with an in-pixel buried-channel source-follower is presented. Compared to a conventional surface-mode source-follower design, it achieves: 1) a reduction of more than 50% in dark random noise and improvement of noise spread; 2) a significant reduction of the RTS noise component; 3) a nearly 100% improvement in pixel output swing; and 4) an increase in voltage gain of the in-pixel source follower.

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References

[1] M.Cohen, F. Roy, D. Herault et.al, "Fully Optimized Cu Based Process with Dedicated Cavity Etch for 1.75μm and 1.45μm Pixel Pitch CMOS Image Sensors," *IEDM Tech. Dig*, pp.127-130, 2006.

[2] Assaf Lahav, D. Veinger and A. Fenigstein, "Optimization of Random Telegraph Noise Non Uniformity in a CMOS Pixel with a Pinned-Photodiode," *Int'l Image Sensor Workshop*, pp. 230-234, June 2007.

[3] K. Findlater, R. Henderson, D. Baxter et al., "SXGA Pinned Photodiode CMOS Image Sensor in 0.35μm Technology," *ISSCC Dig. Tech. Papers*, pp. 218-219, 2003.

[4] Xinyang Wang, P. R. Rao, A. Mierop et al., "Random Telegraph Signal in CMOS Image Sensor Pixels," *IEDM Tech. Dig*, pp.115-118, 2006.

[5] B. Pain, T. Cunningham, B. Hancock et al., "Excess Noise and Dark Current Mechanisms in CMOS Imagers," *IEEE Workshop on CCD and Advanced Image Sensor*, pp.145-148, June 2005.

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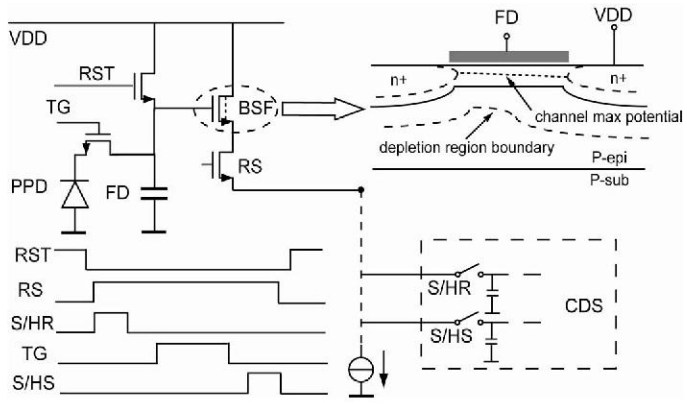

Figure 2.10.1: Pixel structure, basic readout timing and cross section of the BSF.

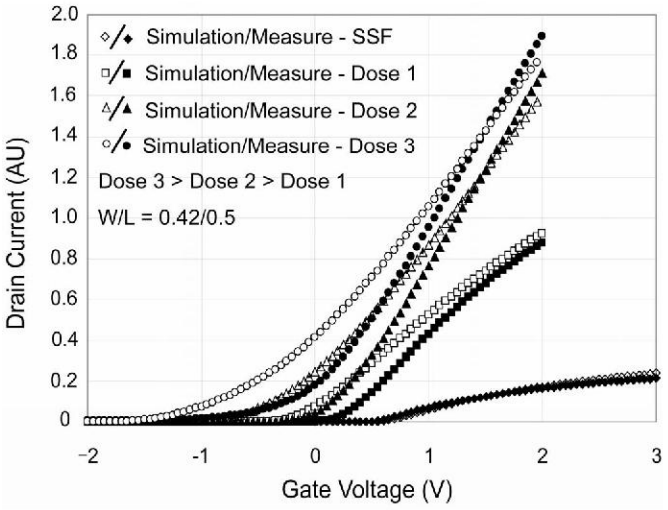

Figure 2.10.2: Gate characterization of buried/surface channel transistors.

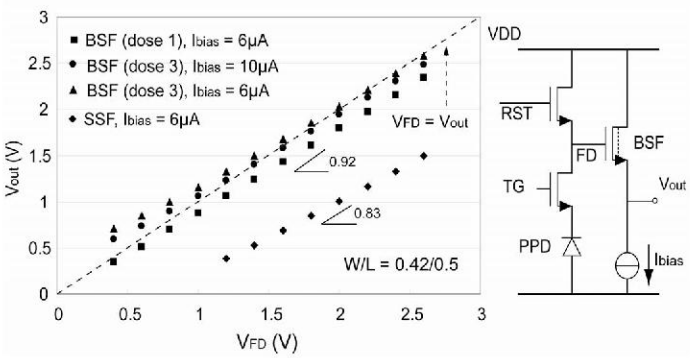

Figure 2.10.3: Pixel test structure and DC measurement results, the dashed line indicates where the BSF's gate voltage equals its source voltage.

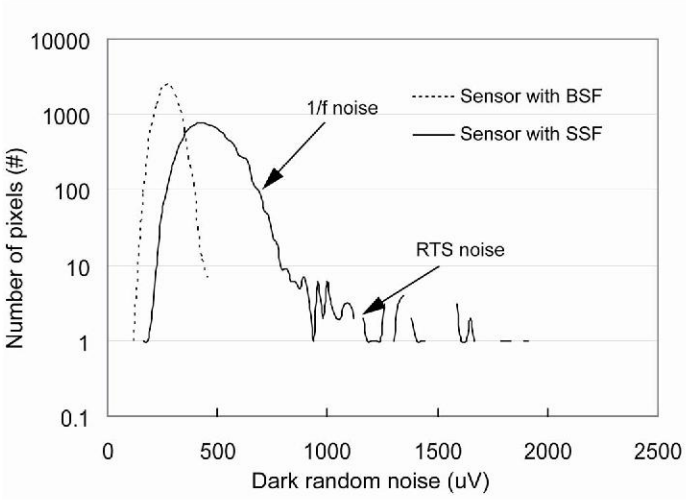

Figure 2.10.4: Measured histogram of dark random noise.

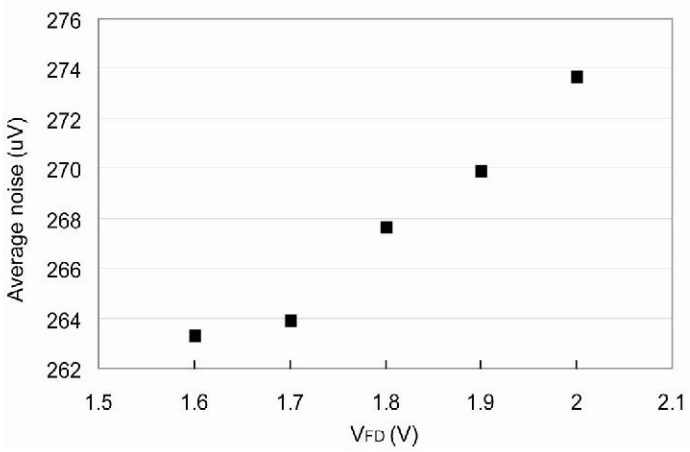

Figure 2.10.5: Dependence of random noise on FD voltage.

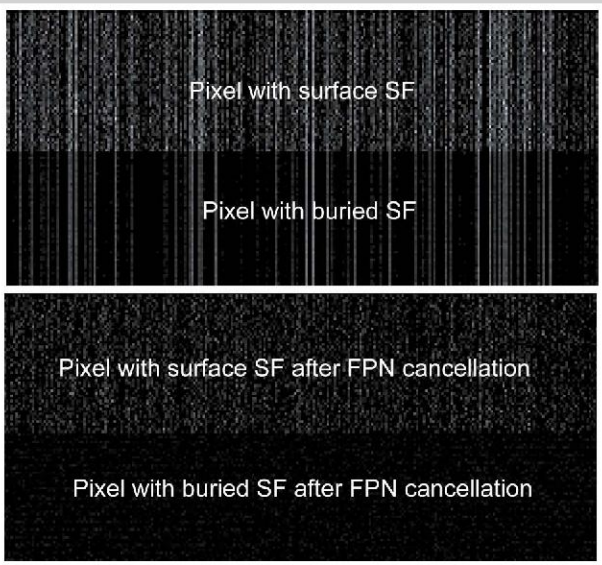

Figure 2.10.6: Test image in the dark, 10× sensor gain.

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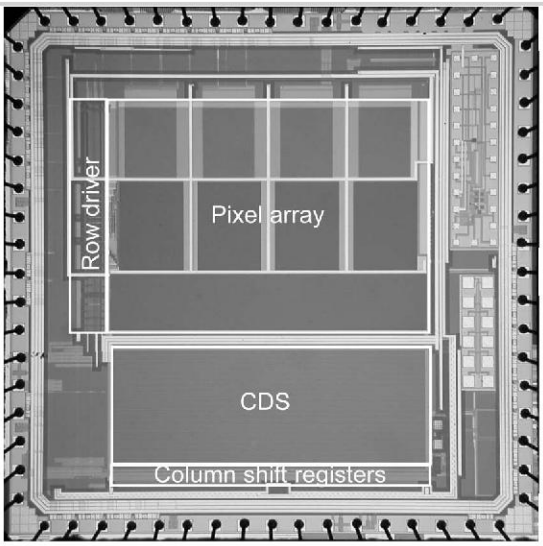

Figure 2.10.7: Chip micrograph of the prototype image sensor. The die size is 4.95mm×4.95mm.

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