

# An Autonomous Low Power High Resolution micro-Digital Sun Sensor

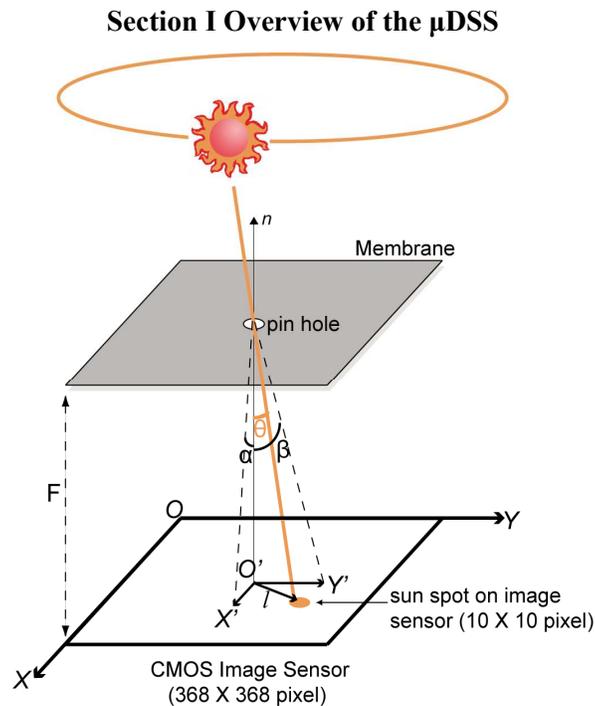
Ning Xie<sup>1</sup>, Albert J.P. Theuwissen<sup>1,2</sup>

1. Delft University of Technology, Delft, the Netherlands; 2. Harvest Imaging, Bree, Belgium;

## ABSTRACT

Micro-Digital Sun Sensor ( $\mu$ DSS) is a sun detector which senses the respective angle between a satellite and the sun. It is composed of a solar cell power supply, a RF communication block and a CMOS Image Sensor (CIS) chip, which is called APS+. The paper describes the implementation of a prototype of the  $\mu$ DSS APS+ processed in a standard  $0.18\mu\text{m}$  CMOS process. The  $\mu$ DSS is applied for micro or nano satellites. Power consumption is a very rigid specification in this kind of application, thus the APS+ is optimized for low power consumption. This character is realized by a specific pixel design which implements profiling and windowing during the detection process. The profiling is completely fast and power efficiently by a “Winner Take ALL (WTA)” principle. The measurement results shows that the APS+ achieves a reduction of power consumption by more than a factor 10 compared to state-of-the-art. Besides the low power consumption, the APS+ also proposes a quadruple sampling method which improves thermal noise with 3-T Active Pixel image Sensor (APS) structure.

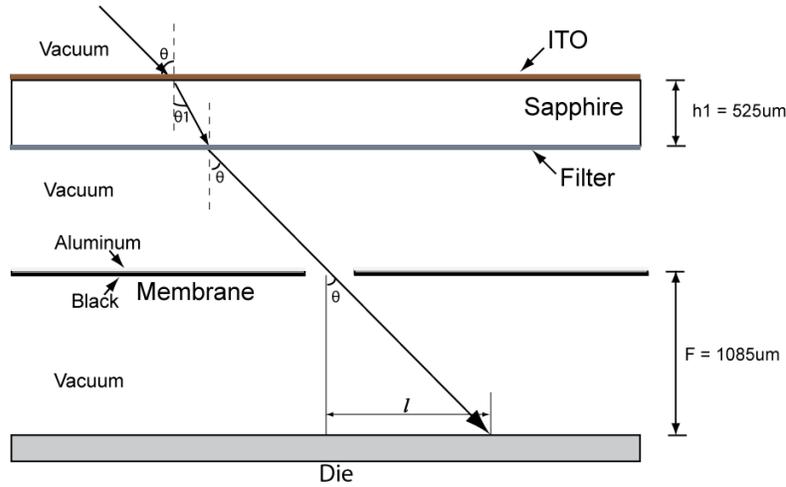
**Keyword list:** CIS, WTA, low power, quadruple sampling, APS



**Figure 1 System sketch of the  $\mu$ DSS**

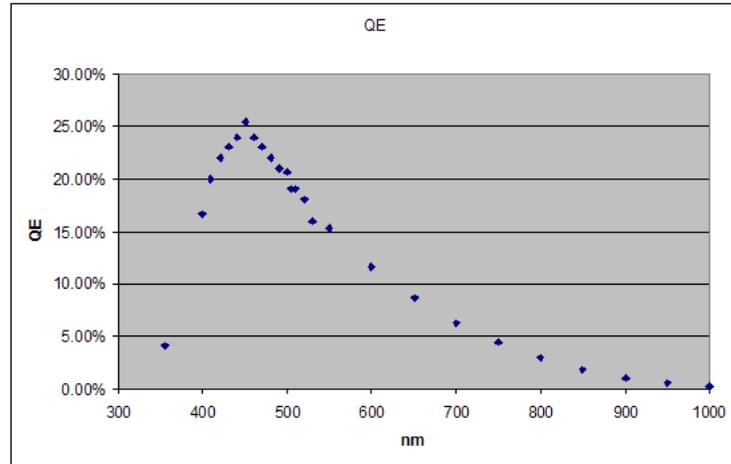
The system sketch of the  $\mu$ DSS [1] is presented in Figure 1. It is a pinhole camera in principle: a CMOS image sensor as the photosensitive component, and a pinhole as aperture. In this application, the sun is considered as a point light

source. A membrane which completely shields the sun light locates above the image sensor's focal plane. A pinhole is at the center of this membrane. The sun light projects an image on the image sensor's pixel array through the pinhole. By reading out the centroid of the sun light projected image, the sunlight incident angle ( $\theta$ ) can be calculated. The satellite's attitude angle  $\alpha$  and  $\beta$  can also be further determined according to the centroid information.



**Figure 2 Sun ray tracking route in the  $\mu$ DSS**

The optical structure of the  $\mu$ DSS is illustrated in Figure 2. A sapphire layer is located on top of the membrane, with a filter at its back side. Without a filter, the pixels will be constantly saturated by the sun light reaching the  $\mu$ DSS surface, since the light intensity has a typical value of  $1500 \text{ W/m}^2$ . The filter will limit the sun light to a reasonable level that the pixels illuminated by the sun light are close to saturation level. This filter has to be designed according to the quantum efficiency of the pixel. The measurement result of the quantum efficiency is presented in Figure 3.



**Figure 3 Measurement results of quantum efficiency**

As shown in Figure 2, an indium tin oxide (ITO) layer is deposited on top of the sapphire window. The ITO layer is a transparent conducting oxide layer, which is connected to the grounded housing. With the ITO layer the charge generated due to cosmic radiation will be discharged through the housing. An aluminum layer is deposited on the top of the membrane; while it is black coated on the bottom side. In this way, the influence from the reflected light will be minimized.

The incident angle  $\theta$  can be achieved by the relation below:

$$l = \tan\theta \times F \Rightarrow \theta = \arctan\left(\frac{l}{F}\right) \quad (E1)$$

Here,  $l$  is the distance between the center of the pixel array and the centroid of the sun spot,  $F$  is the focal length. This relation also shows that the centroiding accuracy is highly decided by the accurate knowledge of the sun spot location on the pixel array.

## Section II Component Structure of the $\mu$ DSS

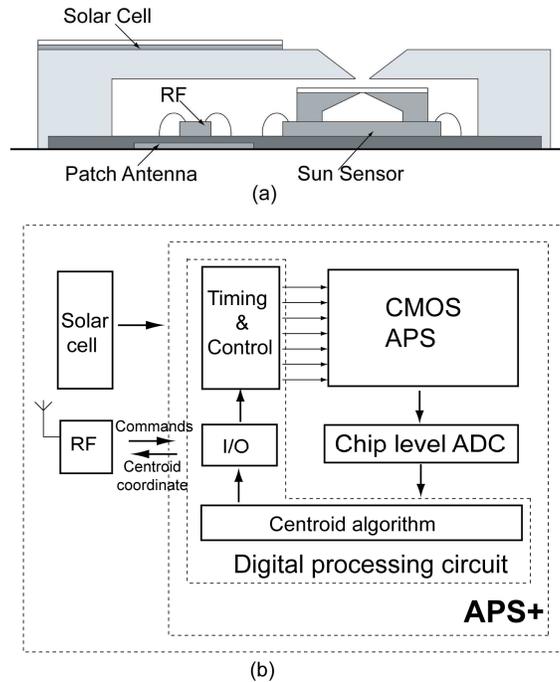


Figure 4(a) Cross section of the  $\mu$ DSS system; (b) Block diagram

Figure 4 illustrates the cross section and block diagram of the  $\mu$ DSS system. As indicated in the block diagram, the  $\mu$ DSS is composed of an image sensor chip named APS+, a solar cell, and an RF module.

The critical component in the  $\mu$ DSS is APS+. It is composed of an APS image sensor, an A-to-D converter (ADC) and digital processing circuit. The functions of these blocks are listed below:

- 1) APS: The APS is the photosensitive element in the system. It converts the incoming light signal into voltage signal. The APS is composed of the pixel array, sample-hold array and readout circuit. The output signal is read out in analog domain.
- 2) Chip level ADC: A 12-bit pipeline ADC is implemented. It reads out the analog signal from the APS and outputs the digital signals to the centroid algorithm circuit.
- 3) Digital processing circuit: The Digital processing circuit includes the centroid algorithm circuit, the I/O interface circuit and Timing and Control circuit. The centroid algorithm determines the sun light projected image's centroid coordinate on the focal plane based on the APS's outputs. Through the I/O interface, the  $\mu$ DSS receives commands from the outside and outputs the centroid coordinate. The Timing & Control circuit generates the timing and control signals for the APS.

Besides the APS+, the solar cell is the power supplier of the system, and the RF block works for communication between the  $\mu$ DSS system and other elements on the satellite.

### Section III Low Power Approach

Due to the small size, the solar cell which can be carried by a microsatellite is relatively small. So the rigid power consumption budget is one of the critical technical challenges for the  $\mu$ DSS.

As indicated in Figure 1, in the  $\mu$ DSS system, the size of the sun spot is approximately  $10 \times 10$  pixels, while the size of the image sensor pixel array is  $368 \times 368$  pixels. The conventional readout method determines the sun spot centroid based on the readout result of the complete pixel array [2]. Under a certain frame rate the high working frequency of ADC and readout circuit results in very high power consumption. In addition, the size of the sun spot is extremely small compared to the whole pixel array. The conventional method wastes most of time and power on reading out the pixels that don't have any useful information. Due to the above reasons, the power consumption of a conventional digital sun sensor can be the order of several watts [2].

The discussion above shows that power consumption reduction can be achieved by lowering down the working frequency for ADC and readout circuit as well as detecting the Region of Interest (ROI) on the pixel array. Both of the targets are realized by APS+. The APS+ adopts a power saving two step acquisition - tracking readout method. Once powered on, the APS+ works in sun acquisition mode in order to detect the coarse location of the sun spot. At the end of the acquisition, the APS+ determines the ROI by evaluating the intensity profiles in column and row directions. In the next step, the APS+ starts working in sun tracking mode: All pixels in the ROI are readout and the final centroid is extracted by the digital algorithm.

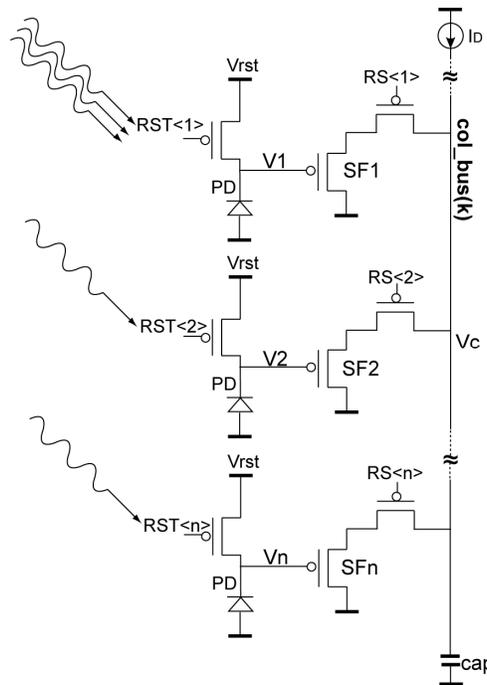


Figure 5 Pixel structure which implements WTA principle

Figure 5 illustrates the pixel structure which implements the WTA principle in the sun acquisition mode [3]. The pixel is structured based on 3-T APS, but with all p-MOS transistors. Assuming the first photodiode is the most heavily illuminated on a specific column, at the end of integration, V1 will be the lowest among all photodiode output voltages (V1, V2... Vn). Right after the integration, all pixels on the same column are shorted on the column bus, the column bus voltage Vc will reduce due to the current floating through the source followers (SF1, SF2... SFn). Vc will keep decreasing until it reaches the value that only SF1 is still in the saturation region, and all other source

followers are turned off. In other words, the column bus voltage is decided by the output voltage of the most illuminated pixel or the so called “winner”. The column profiling is achieved by shortening all row select transistors (RS<1>, RS<2>... RS<n>) during “column profiling” period.

The column voltage is exclusively decided by the “winner” pixel only when the voltage difference between the “winner” and other competitors is larger than a minimum value. This minimum value can be defined as the resolution of the WTA principle. In an ideal case, assume that in the column of Figure 5, the first photodiode is so strongly illuminated that only SF1 is turned on and completely occupies the column current source  $I_D$ . The value of  $I_D$  is selected in the way that SF1 is in the saturation region. The value of  $V_C$  can be derived:

$$V_c = V_1 + V_{TH} + \sqrt{\frac{2I_D}{\mu C_{OX} \frac{W}{L}}}, \quad (E2)$$

here  $\mu$  is the mobility coefficient of holes for p-MOS transistor,  $C_{OX}$  is the gate oxide capacitance per unit area,  $W$  and  $L$  are the width and length of the source follower respectively,  $V_{TH}$  is the threshold voltage. In this result, only first order approximation is used for simplification, the body effect is not considered.

Since only SF1 is active, SF2 (as well as all other source followers) should be turned off, thus we get another relation:

$$V_c - V_2 < V_{TH}, \quad (E3)$$

Combining E2 and E3, the relation between  $V_1$  and  $V_2$  can be achieved:

$$V_2 - V_1 > \sqrt{\frac{2I_D}{\mu C_{OX} \frac{W}{L}}}, \quad (E4)$$

$$V_2 - V_1 > \sqrt{\frac{2I_D}{\mu C_{OX} \frac{W}{L}}},$$

Equation

(E4) shows the minimum difference required between  $V_2$  and  $V_1$  in

order to make sure only SF1 is active, which is the resolution of this WTA circuit. Once several competitors have similar output voltages with difference smaller than this value, it means there is no unique “winner” anymore. Instead several source followers share the total current. If the number of “winners” is increased, the current floating in each source follower will decrease so that some of or even all of the source followers will work in the triode region. Therefore, in practice, since the sun light intensity is very similar within the sun light spot, the column voltage will not be decided by a unique “winner”. However since the number of “winners” is limited by the size of the sun spot, the practical result achieved by WTA can still approximately present the real profiling.

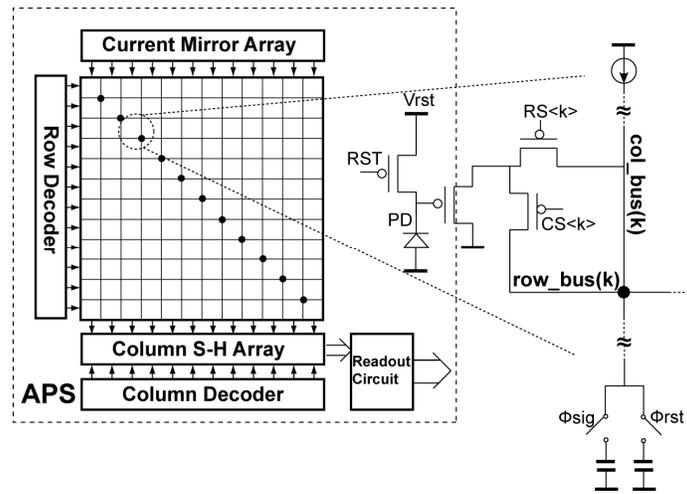
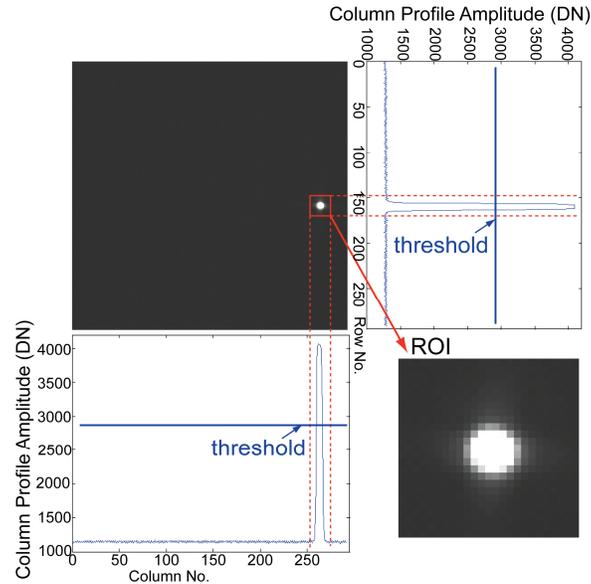


Figure 6 Structure of APS and pixel

In order to achieve the profiling on the row direction, in each pixel extra column select transistor (CS<k>) is required besides the ordinary row select transistor, as indicated in Figure 6. During “row profiling” period, row

profiling output on each row needs to be read out by extra row readout circuit. In order to further simplify the readout circuit, the pixel array is modified. The column and row buses are short cut at the positions of the diagonal pixels (as the dots indicate in Figure 6). In this way the row profiling information is shared by both column and row buses. So the row profiling could be read out on the column buses. No extra readout circuit is necessary for row buses anymore. The measurement result of profiling is presented in Figure 7.

With profiling method, column and row profiles are achieved within the readout time for two lines. This short readout time leads to ultra-low power consumption in the acquisition mode, which is 21.34mW @10fps.



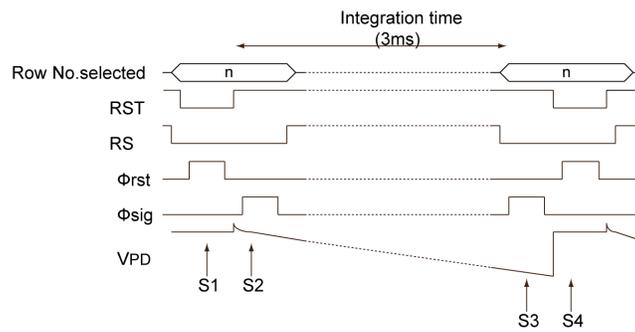
**Figure 7 Measurement results from acquisition mode and tracking mode**

#### **Section IV. Low noise approach**

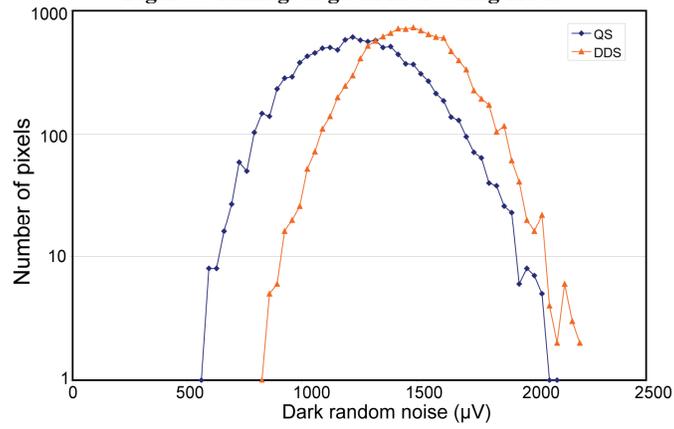
In the sun tracking mode, the final centroid result is extracted. Therefore low noise is the major consideration in this mode. The 3-T pixel structure is required by the WTA principle. The drawback is the reset noise is relatively higher than 4-T pixel structure. In order to reduce the kTC noise, the APS+ employs a readout strategy called “quadruple sampling”. The timing diagram is depicted in Figure 8 (control nodes are indicated in Figure 6). Four samples are taken in one readout cycle. Samples S1 and S4 are taken when RST is active; S2 and S3 are taken at the beginning and end of integration time, respectively. The kTC noise components in S2 and S3 are correlated, and can be cancelled by subtracting. During the quadruple sampling, firstly the subtractions of S1-S2 and S4-S3 are processed in the analog domain in order to cancel 1/f noise, and the results are digitally stored on chip. Next, the digital outputs of the previous actions are subtracted in order to cancel the kTC noise. In the end, the final output is  $(S4-S3)-(S1-S2) = S2-S3$ . In this result, the 1/f noise and kTC noise, being the major noise contributions, are cancelled. The measurement result is presented in Figure 9. Both the quadruple sampling and the conventional delta double sampling (DDS) are applied to APS+. It shows that quadruple sampling achieves 15% less thermal noise than DDS.

#### **Section V. Performance**

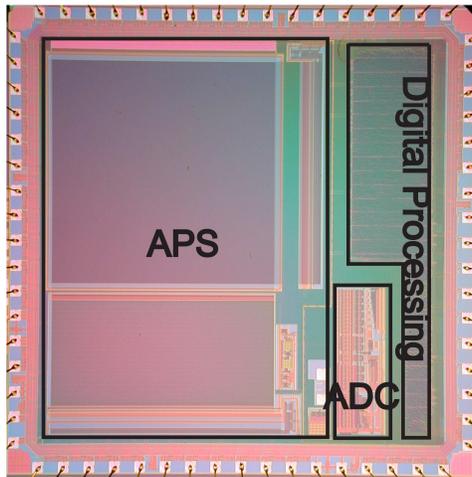
The comparison between the presented work and other recently reported sun sensors are listed in Table 1. It clearly shows the improvements in power consumption, chip size, accuracy, and resolution. The micrograph of the APS+ is presented in Figure 10.



**Figure 8 Timing diagram in tracking mode**



**Figure 9 Histogram of dark random noise with Quadruple Sampling (QS) and Delta Double Sampling**



**Figure 10 Micro graph of APS+**

μDSS vs. counterparts	Characteristic	μDSS (This work)	Galileo (ESA) [4]	SS-411 [5]
	Year	2010	2010	2009
	Chip Size	5mm ×5mm	11mm ×11mm	Not available
	Pixel Array	368 × 368	512 × 512	Not available
	Power Consumption	21.34mW @Acquisition 21.39mW@Tracking	327mW @ Acquisition 193mW @ Tracking	75mW
	Power Supply	3.3V for analog 1.8V for digital	3.3V for analog 1.8V for digital	5V
	FOV	±47°	±64°	±70°
	Operating Temperature	-40°C to +80°C	-40°C to +70°C	-25°C to +70°C
	Accuracy	0.02° (3σ)	0.024° (3σ)	0.11° (2σ)
	Resolution	0.004°	<0.005°	Not available
	Detection Principle	Single pin hole	Single pin hole	Multiple-apertures

**Table 1. Performance comparison between the μDSS and the state of the art**

#### Reference

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