Charge Domain Interlace Scan Implementation in a CMOS Image Sensor

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***Abstract*—This paper presents the first CMOS image sensor which implements a charge domain interlacing principle to improve the signal-to-noise ratio (SNR) under equal exposure condition (integration time and light intensity). Inspired by the shared amplifier pixel structure, a novel pixel is designed to fit the charge domain interlacing principle, which works in field integration and frame integration mode. The designed image sensor is implemented in TSMC 0.18 μm CIS technology. This CMOS image sensor also contains a programmable universal image sensor peripheral circuit, allowing this sensor also to support normal progressive scan. By comparing the performances of the sensor working in charge domain interlacing and in the progressive scan, the chip measurement results prove that under the same exposure condition, the light response of the charge domain interlacing is twice that of the progressive scan. The SNR performance can be increased by 6 dB in low light level conditions.**

***Index Terms*—Charge binning, CMOS image sensor, interlace scan, low light level imaging.**

I. Introduction

DURING the past few years, fueled by the demands of multimedia applications, digital still and video cameras have become very popular and are used widely. The image sensor which is the key component in modern digital cameras, converts the light intensity to electric signals. The CMOS image sensor technology has made outstanding progress and has some distinct advantages such as power consumption, cost, and integration level. Nevertheless, there are still some performance constrains for CMOS image sensor technology when compared with CCD technology [1]. For example, CMOS Active Pixel Sensor (APS) has lower sensitivity when compared to CCD because the former has limited fill factor and lower quantum efficiency. Further, CMOS image sensors also suffer from several fixed-pattern noise sources especially under low illumination conditions. To improve the overall image quality, high SNR performance and high dynamic range (DR) are desired. Retrospect the history of the CMOS image sensor development, the literature review shows that to achieve high SNR, most researchers try to reduce the noise. For instance, the APS [2] technology was designed to achieve a lower readout noise, and an improved scalability to large array formats. The pinned photodiodes (PDs) in a four transistors (4T) pixel along with the column level correlated double sampling (CDS) reduces the reset noise (kTC) generated by the reset action in the pixel and the fixed pattern noise. All of these technologies improve the SNR by reducing different noise sources. Beside noise reduction, the SNR can also be improved by enhancing the signal level under equal exposure conditions (exposure time and light intensity) especially for low light level imaging [3]. Preamplifiers with a very high analog gain are commonly used to suppress the noise in the readout electronics [4]–[6].

In this paper, we present a CMOS image sensor which increases the signal level by using a charge domain interlacing principle. To the best knowledge of the authors, this is the first time that the charge domain interlace principle is implemented in a CMOS image sensor, though it has been already in use in CCDs.

This paper is organized as follows. In Section II, the charge domain interlacing principle is introduced and compared with other scan modes in detail. Section III presents the designed image sensor and the newly proposed pixel structure. The pixel structures are specifically designed to implement charge domain interlacing scan in CMOS. The measurement results showing the SNR improvement are shown in Section IV. Finally, this paper ends with conclusions in Section V.

II. Charge Domain Interlacing Principle

A. Interlace Scan and Progressive Scan

The interlace scan mechanism was proposed for conventional TV systems. At that time, it was used because of its small bandwidth advantage compared with progressive scan. Progressive scan means all lines of a video frame are scanned successively. The lines in a progressive image are scanned from one row to the next, from top to bottom. The whole frame is created in one time, which is different for the interlace scan. The interlace scan does not transmit all the lines of a frame in their logical order. Instead, each frame is divided into two parts, an odd field (the image made by odd lines) and an even field (the image made by even lines). The CCDs using the interlacing technology were first introduced by C. Sequin in 1973 [7]. Besides the bandwidth advantage of interlace scan, there are other reasons why interlace scan was chosen for CCD image sensor and even CMOS image sensor nowadays. To better understand these advantages of the interlace scan mechanism, two different readout modes of the interlace scan and the progressive scan are introduced below:

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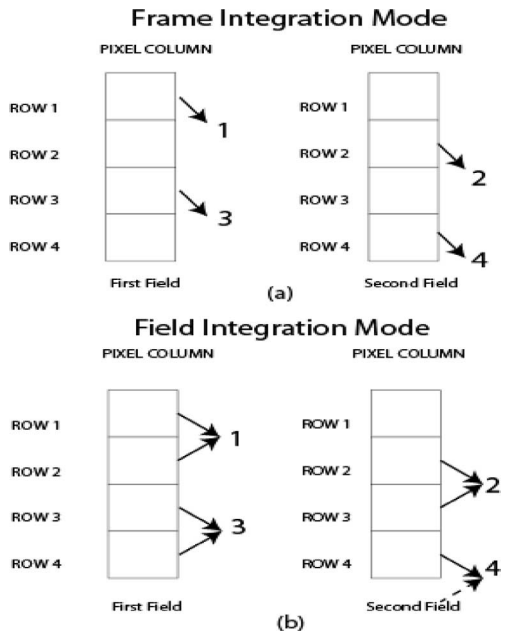


Fig. 1. (a) Diagram of the frame integration mode. (b) Diagram of the field integration mode.

Frame integration mode [Fig. 1(a)]: During the first field, the odd lines $(1,3,5\ldots)$ are scanned and the output is available as line $1,3,5\ldots$ The second field consists of the even lines $(2,4,6\ldots)$, and also output the signal as even lines $2,4,6\ldots$ The SNR and temporal resolution for a CMOS image sensor implementing this frame integration mode is the same as for the progressive scan. The advantage of the frame integration mode is the full spatial resolution defined by the pixel geometry and its easy implementation. Because its integration time is equal to the frame time, it is called frame integration mode.

Field integration mode [Fig. 1(b)]: In this mode, the two adjacent scanning lines are added together. In the odd field, the lines $1+2,3+4,5+6\ldots$ are output as the lines $1,3,5\ldots$ The lines $2+3,4+5,6+7\ldots$ are used to make the even field and output as the line $2,4,6\ldots$ The integration time is the field time which is half of the frame time, so it is called field integration mode. When compared with frame integration mode, the double signal level in the interlace modes can achieve a higher light sensitivity when compare under the equal integration time.

Progressive scan: Means all lines of a video frame are drawn in sequence, and each field has the same number of lines as a frame. The whole frame is created in one time, which is different from interlace scan.

The characteristics of the above mentioned scan modes are summarized in the Table I. Because the field integration mode combines two scanning lines together, this is equal to enlarge the pixel size two times and means a better light sensitivity [8] compared to progressive scan. The characteristics of the field integration mode can be summarized as follows. First, no field time lag is present [9]. Due to the shorter integration time for the field integration mode, the time delay between two images (called "field time lag") is much less than in the case of the frame integration mode. Second, it is reducing the flicker at vertical edges in the image since the field integration mode doubles the vertical aperture. Third, the vertical resolution of the field integration mode is lower than in the case of progressive scan and frame integration mode. Lastly, but not least, it has a higher sensitivity compared to the frame integration mode or progressive scan when the integration time is the same. In this situation, the high temporal resolution of the field integration mode will be traded off with the high sensitivity advantage.

TABLE I
DIFFERENT SCAN MODES COMPARISON

	Field integration mode	Frame Integration mode	Progressive Scan
Sensitivity	200%	100%	100%
Temporal resolution	high	low	high
Spatial resolution	about 70%	100%	100%

The above analysis shows that interlace scan was used because of its good compromise between spatial and temporal resolution and reduction in the flicker on one hand, while small bandwidth on the other hand. However, here we choose it because the image sensor could achieve a better light sensitivity when the field integration mode interlace scan is implemented.

B. Charge Domain or Voltage Domain

To realize the field integration mode interlace scan, the most convenient way is the addition of the pixel signal in the voltage or even in the digital domain. This method is similar with adding an amplifier $(\text{gain}=2)$ after the pixel readout [10]. In this situation, the signal level will be doubled truly, however, adding the signal in the voltage domain comprises the summation of all noise sources from the whole sensor readout chain and will have a negative effect on the final SNR compared with the charge domain signal summation. On the other hand, the SNR improvement in the voltage domain using a preamplifier is not significant in low light levels, when the readout noise is dominating compared to the charge domain mode of operations. A better method of field integration mode interlace scan realization is the charge domain interlacing principle, which is based on the charge binning method. Since the signals are added in the charge domain before readout, the total readout noise floor is not affected by the signal summation at all. Thus, when the readout noise is dominated in low light level, a higher SNR is achieved in charge domain than the interlacing method in the digital domain. The mathematical proof is given in the following.

The different SNR performances of the charge domain interlace scan, normal progressive scan, and digital domain interlace scan are described in (1)–(3), respectively. Equation (4) shows the improvement in SNR when the progressive scan is replaced by charge domain interlaces scan. Equation (5) compares the SNR improvement between charge domain and digital domain

$$\begin{aligned}\text{SNR\_charge} &= 20\log\left(\frac{2S}{\sqrt{N_r^2+2N_s^2}}\right)\\ &= 20\log\left(\frac{2S}{\sqrt{N_r^2+2S}}\right)\end{aligned} \tag{1}$$

$$\text{SNR\_progressive} = 20\log\left(\frac{S}{\sqrt{N_r^2+N_s^2}}\right) = 20\log\left(\frac{S}{\sqrt{N_r^2+S}}\right) \quad (2)$$

$$\text{SNR\_digital} = 20\log\left(\frac{2S}{\sqrt{2N_r^2+2N_s^2}}\right) = 20\log\left(\frac{2S}{\sqrt{2N_r^2+2S}}\right) \quad (3)$$

$$\text{SNR\_charge} - \text{SNR\_progressive} = 20\log\left(2\sqrt{\frac{N_r^2+S}{N_r^2+2S}}\right) \quad (4)$$

$$\text{SNR\_charge} - \text{SNR\_digital} = 20\log\left(\frac{\sqrt{2N_r^2+2S}}{\sqrt{N_r^2+2S}}\right) \quad (5)$$

In all equations, N_r is the input-referred noise coming from the readout circuit, and N_s is the photon shot noise of the signal, which has the square-root relationship with the signal S itself in charge domain ($N_s = \text{sqrt}(S)$). All parameters are expressed in number of electrons. From (4), we can derive that for low light levels ($N_r \gg N_s$) the charge domain interlace scan gives a maximum of 6 dB improvement compared to progressive scan, in the photon shot noise dominated part ($N_r \ll N_s$), the improvement is 3 dB. From (5), it can be found that, in low light level conditions, when the readout noise is the dominate noise source, the charge domain interlace will have 3 dB advantage compared with digital domain interlace. In the photon shot noise dominated part, these two binning technologies will have the same performance.

The analysis above explains the reasons for the increase in the signal level and SNR in the charge domain interlacing principle. To experimentally verify the charge domain interlacing principle for CMOS image sensors, we proposed two pixel structures that allow summation of the photon generated electrons of two pixels in charge domain. The binning technology in the charge domain is based on the idea of sharing the readout circuitry among pixels. In 2004, Matsushita *et al.* [11] and Takahashi *et al.* [12] both presented pixels with shared readout circuits. The concept of sharing the readout circuit by four adjacent pixels is a time-division multiplex readout. These shared readout structure were proposed to obtain small pixel pitches with a high fill factor. Here, we use a similar structure to realize the charge binning technology in the pixel.

III. Sensor Implementation

In the previous section, the working principle of the charge domain interlacing principle was explained in detail. In this section, the circuit level implementation of the charge domain image sensor is presented.

Fig. 2 shows the architecture of the sensor, which contains the pixel array, the current source array, the column multiplexer, the CDS circuitry, the row/column driver array, the programmable pulse generator, a gray code counter and the an output buffer.

The charge domain interlacing scan principle has been implemented in a CCD image sensor, because the charge-coupled device is naturally suited for charge domain operation. However, for the CMOS image sensor technology, the normal 4T pixel structure cannot realize the charge binning operation. Inspired by the shared amplifier pixel structure, this paper proposes a pixel structure [Fig. 3(a)] based on the pinned-photodiode (PPD) 4T structure. In the field integration mode, each row will be scanned twice both for the odd field and the even field, not only the readout structure will be shared by two PDs (1, 2) placed in two different rows, but also the individual PDs (2) will be connected and readout by two neighboring readout structures $(1', 2')$. In the odd field scan, electrons accumulated in PDs 1 and 2 are transferred to one common floating diffusion (sense node, a special capacitance to store and read the photon produced electrons) by turning on $T1\langle 0\rangle$ and $T2\langle 0\rangle$ at the same time. The corresponding output voltage $1'$ is the combination of the signal produced by PDs 1 and 2. In the even field, electrons accumulated in PDs 2 and 3 are transferred and readout together in $2'$. This proposed two-photodiodes-shared-one-readout pixel structure adds one more transfer gate for one pixel (photodiode) which results in five transistors per pixel (photodiode). For this reason, the fill factor is lower than normal 4T pixel. The proposed pixel design perfectly and naturally matches the field integration mode in the charge domain which is equal to doubling the pixel size.

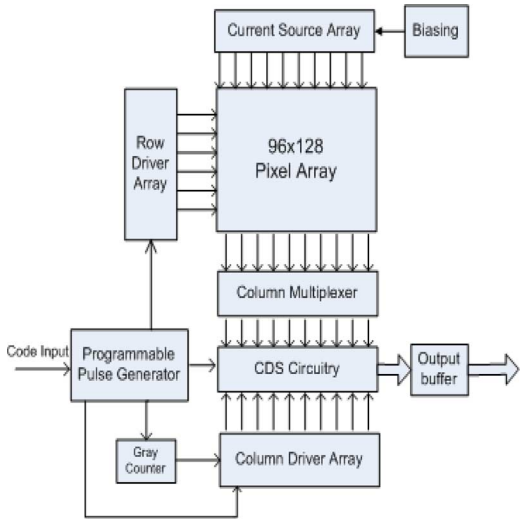


Fig. 2. Architecture of charge domain interlacing CMOS.

Based on the same idea, there is another pixel type [Fig. 3(b)], which is also suitable for the charge domain interlace principle. This structure is using three PDs sharing one readout structure and the readout structure is reused in the odd and the even field [10]. For this structure, every odd numbered photodiode (1, 3, 5) is connected with two transfer gates like photodiode 3 was connected to transfer gates $T2\langle 0\rangle$ and $T1\langle 1\rangle$. All of the transfer gates T2 are used in the even field readout, and all T1 are used in transfer charges in the odd field readout. T1 and T2 belong to two readout circuits, respectively. The even numbered photon sense elements (like photodiode $2, 4, 6\ldots$) are not shared but belong to one particular pixel readout circuit, no matter the odd field scan or even field scan. Every even numbered photodiode (2, 4) is only connected with one transfer gate T3, which will

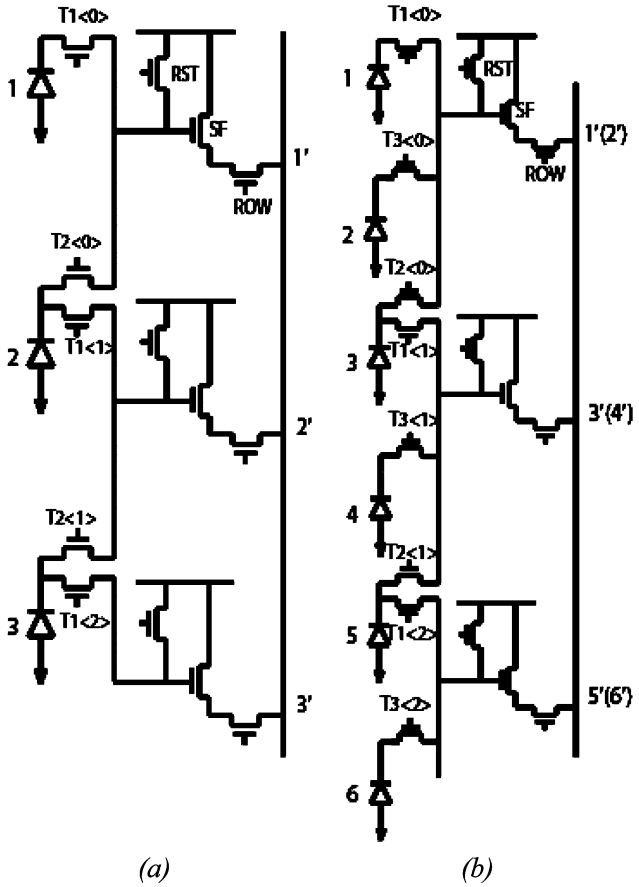


Fig. 3. Proposed two/three PDs shared pixel structure.

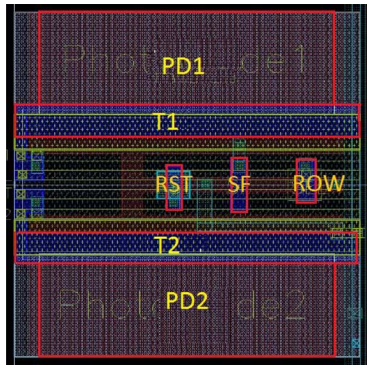


Fig. 4. Two PDs shared amplifier pixel layout.

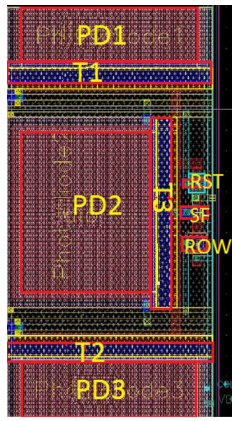


Fig. 5. Three PDs shared amplifier pixel layout.

be used for charge transfer control in both fields. This structure will increase the fill factor compared with the pixel of two PDs sharing one readout structure. Both of these two structures can combine the signals in the charge domain at the front-end and not in the voltage domain or digital domain, and these two structures can also be used in the progressive scan without the sensitivity benefit.

Compared with the structure in Fig. 3(b), the advantage of the two PDs shared pixel structures is its higher level of symmetry, easily implementation and it has a smaller floating diffusion capacitance which consequently provides a larger conversion gain.

The pixel array designed contains these two types of pixel designs. Both basic pixels pitches in one row are 10 μm $\times$ 10 μm. From rows 0 to 62, the two PDs shared amplifier pixel structure (Fig. 4) is used. The fill factor for this pixel structure is 46.4%. The fill factor will decrease further with the pixel pitch shrinking. From rows 63 to 124, the three PDs shared amplifier pixel structure (Fig. 5) is used. The fill factor is 47.8%. One pixel structure was reused in two rows, so the structure size is 10 μm $\times$ 20 μm. The pixel design should consider two aspects, first of all, the symmetry requirement. Because these pixels charge domain interlacing, some PDs will be shared by different readout circuits and charges stored in one photodiode will be transferred in two opposite directions in different fields. Thus, the two PDs shared one readout circuit pixel structure (Fig. 4) should be fully symmetric with respect to the readout structure of the pixel. For three PDs shared one readout circuit structure (Fig. 5), the PD2 is just connected with one transfer gate (T3) and a floating diffusion. But the other two photodiodes (PD1 and PD3) are connected with two transfer gates and two floating diffusions. In this situation, the layout of these three PDs is hard to be exactly the same with each other. However, on the other hand, if we consider the charge domain interlacing aspect, the PD1 and PD2 add together as a readout unit, PD2 and PD3 add together as a readout unit, these two units will be symmetric when PD1 and PD3 are symmetric to PD2. To keep the symmetry of the layout for three PDs shared pixel structure, a dummy metal line to control the transfer gate (T3) is added. Secondly, to reduce the kTC noise and optimize the conversion gain, the capacitance of the floating diffusion should be small. Specially, for these shared PDs pixel designs, the floating diffusion which connected with more than one photodiode normally is larger than for a normal pixel. Thus, we should try to control the area of the floating diffusion to improve the conversion gain. The kTC noise will be cancelled when CDS technology is applied.

To test this pixel design and the working principle of the interlacing technology, a programmable universal image sensor driving circuit was proposed. This peripheral circuit can drive and readout the pixel array in a flexible, efficient way and easily changes the working mode through a different programming. This sensor can not only support progressive scan, frame integration interlace scan mode, field integration interlace scan in

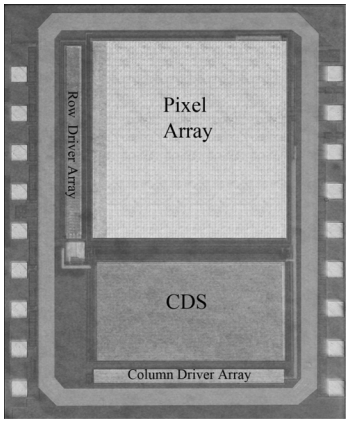


Fig. 6. Chip micrograph of the test image sensor.

TABLE II
CHIP SPECIFICATION SUMMARY

Specification	Value
Process	TSMC 0.18μm 1P4M CIS
Power Supply	3.3 V (A) /1.8V (D)
Area	2.3mm ×2.7mm
Pixel Pitch	10μm ×10μm
Pixel Array	82×124

voltage domain, but also can realize the charge domain interlacing principle. This is a unique feature of this CMOS image sensor.

IV. MEASUREMENT RESULTS

The test sensor was fabricated in a 0.18-μm 1P4M CMOS process by TSMC. The chip micrograph with several fundamental functional blocks of the prototype chip indicated is shown in Fig. 6. The output of the image sensor is an analog signal, being converted into a digital signal by an off-chip 12 bit ADC. The sensor specification is listed in Table II.

To measure this chip and prove the theory and principle we proposed, first, we compare the noise performance of the charge domain interlace scan with normal progressive scan. The signal-variance analysis is a powerful tool to measure the image sensor noise performance. In the sensor signal-variance analysis of Fig. 7, the plots for the two PDs shared pixel structure in progressive scan and interlace scan coincide with each other. It is the same situation for the three PDs shared pixel structure. Thus, the two PDs shared pixel structure has the same conversion gain (slope) of 0.0146 DN/e$^-$ in both scan modes. This result shows that under an equal signal readout level, the image sensor working in.

Second, to prove that the charge domain interlace scan can improve the light sensitivity of the image sensor, Fig. 8 compares the light response of the charge domain interlace scan with the progressive scan based on the two PDs shared readout pixel structure. To measure this light response, the light environment is kept constant in the whole measurement. With increasing integration time, the mean pixel signal level linearly increases.

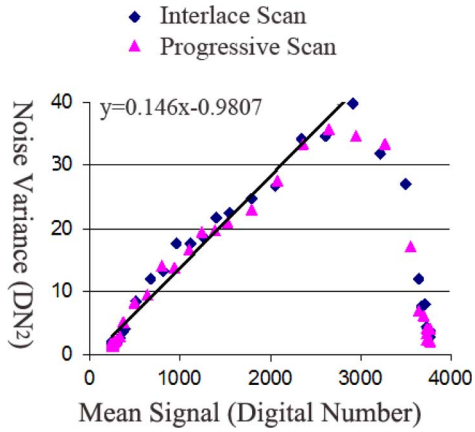


Fig. 7. Noise performance of two PDs shared pixel.

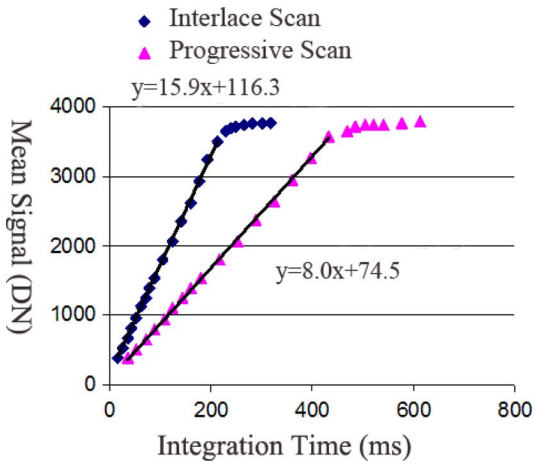


Fig. 8. Light response of progressive scan and interlace scan.

From the slope of these two curves, it can be found that the light response of the charge domain interlace scan is 15.9 DN/ms (1089 e$^-$/ms), which is nearly twice the value of the progressive scan (8.01 DN/ms, 548 e$^-$/ms). This means that under the same light level input and integration time, the average signal level of the interlace scan is twice the value of the progressive scan.

Further, as we mentioned in the beginning of this paper, increasing the signal level under the same exposure condition can improve the SNR. To prove that directly, Fig. 9 compares the charge domain interlace scan with the progressive scan in their SNR performance (this measure is based on the two PDs shared pixel structure). Under the same optical input level, in low light level conditions [0 . . . 100 e$^-$/um^2], the field integration mode interlace scan will improve the SNR by 5–6 dB compared with progressive scan. In this case, the readout noise is the main noise source. When the photon shot noise dominates the noise, the interlace scan can have about 3–4 dB SNR improvement compared with progressive scan. This result confirms the expectation and the analysis of the field integration interlace design.

On the other hand, the original data of the progressive scan can be processed as well to achieve the field integration interlace scan in digital domain. In Fig. 9, the SNR performances of both the charge domain and digital domain interlace scan are

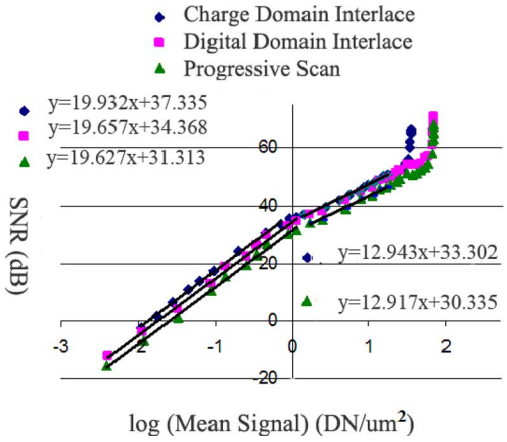
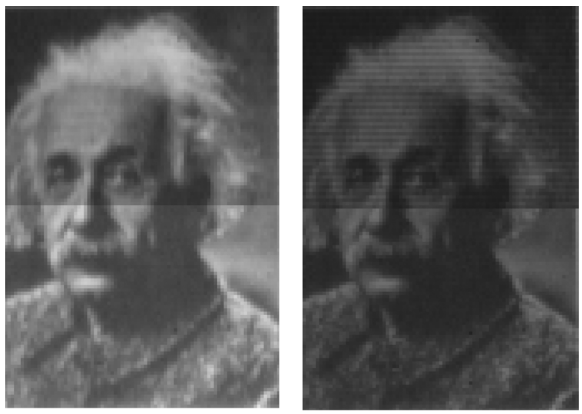


Fig. 9. SNR for two PDs shared pixel interlace scan.



(a) (b)

Fig. 10. Reproduced images from a 82 × 124 pixel array (upper half is three PDs shared pixel array; lower half is two PDs shared pixel array). (a) Charge domain interlace scan. (b) Progressive scan.

compared. Under low light level conditions, the charge domain interlacing improves the SNR by 2.7 dB compared to the digital domain interlacing. With increasing the signal, the SNR is the same for both interlacing methods. Those observations confirm the theoretical studies from the section above.

Finally, two images of the progressive scan and the charge domain interlace scan under the same exposure conditions are shown in Fig. 10. The improvement of the light sensitivity of charge domain interlace scan [Fig. 10(a)] is clearly visible when compared with the progressive scan image [Fig. 10(b)]. Because in the layout of the three PDs shared pixel structure [Fig. 5] the light sensitivity area is a little bit smaller than the two PDs shared pixel structure [Fig. 4], the average signal level of the upper image is lower than lower half of the image. When the sensor is working in progressive scan, due to the nonsymmetry of the three PDs shared pixel layout, we can see the row stripes in the upper part of the image [Fig. 10(b)].

In summary, the measurement results prove that the proposed charge domain interlacing CMOS image sensor can enhance the light sensitivity of the sensor and indeed improve the SNR under the same exposure condition especially for the low light level imaging.

V. Conclusion

The first CMOS image sensor implementing the charge domain interlacing principle has been presented. Before that, the charge domain interlacing principle was only possible for CCD image sensors. From the analysis of the difference between progressive scan and interlace scan, we can conclude that the field integration mode interlace scan sacrifices spatial resolution to achieve a better signal sensitivity. Compared with the normal progressive scan, and digital domain interlacing principle, the test sensor achieves the better SNR performance by enhancing the signal level under the same exposure conditions. A new pixel structure based on the shared amplifier pixel structure was proposed to fit the charge domain interlacing principle. This structure can naturally match the field integration interlace scan in the charge domain, and it makes that the two fields of the interlace scan can perfectly fit and have a spatial offset of one row. The measurement results prove that under the same exposure conditions the charge domain interlace scan can achieve two times the signal value of the progressive scan, which gives an SNR improvement of maximum 6 dB under low light conditions, and about 3 dB improvement when the photon shot noise is becoming the dominant noise source.

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