Column-Parallel Digital Correlated Multiple Sampling for Low-Noise CMOS Image Sensors

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***Abstract*—This paper presents a low-noise CMOS image sensor using column-parallel high-gain signal readout and digital correlated multiple sampling (CMS). The sensor used is a conventional 4T active pixel with a pinned-photodiode as detector. The test sensor has been fabricated in a 0.18 μm CMOS image sensor process from TSMC. The random noise from the pixel readout chain is reduced in two stages, first using a high gain column parallel amplifier and second by using the digital CMS technique. The dark random noise measurement results show that the proposed column-parallel circuits with digital CMS technique is able to achieve 127 $\mu V_{\rm rms}$ input referred noise. The significant reduction in the sensor read noise enhances the sensor's signal-to-noise ratio (SNR) with 10.4 dB. Such sensors are very attractive for low-light imaging applications which demand high SNR values.**

***Index Terms*—4T active pixel sensor, CMOS image sensor, digital CMS, low-light level imaging, low-noise column-parallel circuits.**

I. Introduction

GENERALLY, CMOS image sensors (CISs) for low-light level imaging require a decent low-noise performance. To achieve very low-noise performance at low-light levels, preamplifiers are often used. The preamplifiers usually have very high analog gains and are thus useful to suppress the noise contribution from the following readout electronics [1]–[7]. Another approach is using correlated multiple sampling (CMS) technique to reduce the random noise from pixels and the readout circuits [8]–[11]. However, both approaches fall short in applications like scientific imaging, medical imaging, etc., where usually a very high signal-to-noise ratio (SNR) is desired. Therefore, in order to enhance the SNR of CMOS imagers to meet the requirement for low-light imaging application, certain readout chain circuits with further reduced read noise floor and high-gain amplification are necessary.

Recently column-parallel single slope A/D converters (SS-ADCs) with low bandwidth readout have been presented [11]–[13]. These single slope A/D converters do not use analog output buffers, the noise of which is significant in the overall noise of the signal readout path in CIS. Thus, the use of low-noise high-resolution column parallel A/D converter would improve the low-noise performance of the image sensors. Due to its simple circuit topology, good linearity and noise performance, the SS-ADC is nowadays widely used [11], [12] as column-parallel ADC for CIS. Moreover, with such column-parallel ADCs, a so-called digital CMS approach which performs both of the multiple sampling and processing (generally averaging) in the digital domain is able to be implemented.

This further helps in noise reduction. As already mentioned, for low-light levels, a column amplifier with high analog gain can reduce the random noise, thus effectively increases the SNR [1]–[7].

Therefore, in this paper, we present a new topology of column-parallel circuits using not only a column gain amplifier but also a column ADC for the digital CMS approach to provide the CMOS imager with further reduced low noise and thus enhance its SNR.

The concept, design, and measurement results are presented as following sections. In Section II, the image sensor, the topology of the low-noise column-parallel circuits and their operation principles are described. In Section III, a detailed noise analysis and the noise reduction obtained using the proposed column-parallel circuits is discussed. The noise measurement results from the test chip are shown in Section IV. Finally, the conclusions are outlined in Section V.

II. Design and Principle of Operation

A. Sensor Column Architecture

Fig. 1(a) shows the simplified schematic diagram of the 4T pixel with a pinned-photodiode and the proposed column readout circuits, including a gain amplifier and a SS-ADC. The pixel operation requires three control signals, sensing node reset (RT), photodiode charge transfer (TX), and row select switch (RS), which can be controlled by row decoders. Besides the pixel, the sensor readout chain and the external on-board circuits also contribute to the overall noise of the sensor. The noise from the readout chain is usually dominating in the pixel read noise in wide bandwidth. The use of the column gain amplifier can reduce this large noise by amplifying the signal which will narrow the bandwidth due to the conservation product of gain and bandwidth, before the rest of the read noise is added. The gain here is defined by the capacitance ratio of $C_{\rm in}/C_{\rm fb}$, where $C_{\rm in}$ is the input capacitor, and $C_{\rm fb}$ is the feedback capacitor of column gain amplifier, respectively. The output of the column gain amplifier is connected to the column SS-ADC using an auto-zero capacitor $C_{\rm az}$. The column SS-ADC consists of a comparator, driven by a ramp voltage and a bit-wise inversion

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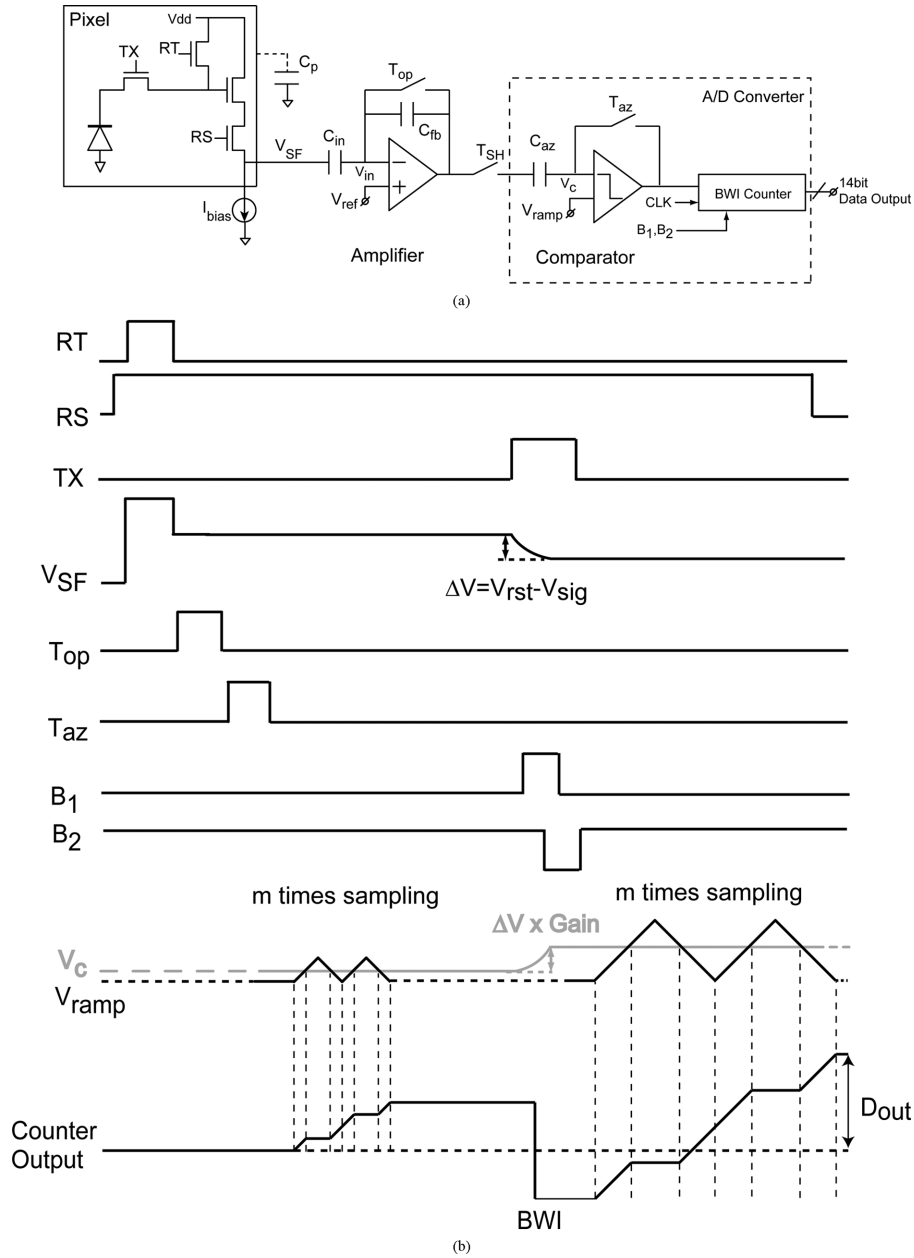

Fig. 1. (a) Schematic diagram of pixel and the proposed column readout circuits. (b) Timing diagram of the column readout chain for digital CMS.

(BWI) counter [14]. The BWI is composed of a ripple counter and BWI cells to perform the A/D conversion by counting the number of clocks until the comparator output changes. The advantage of using a ripple counter is that it does not need to be synchronized, while using a high-speed clock. The BWI counter shows 32% reduction in power consumption and 2.4 times improvement in maximum speed over the conventional up/down counter [14]. After the ADC, the digital output of the sensor is ready to be readout.

B. Principle of Operation

Fig. 1(b) shows the readout timing diagram of the pixel and column readout chain. Initially, the floating diffusion (FD) node of pixel is reset, and then the column gain amplifier and the comparator are reset sequentially as well. The pixel reset transistor (RT), the amplifier reset switch $T_{\rm op}$, and the comparator reset switch $T_{\rm az}$ are closed sequentially. This sequential closing of the reset switches produces a "cascaded noise cancelling" process [6], which isolates the reset noise and offset noise of every previous stage by storing it in a subsequent capacitor and thus be cancelled by the analog correlated double sampling (CDS) later on [6], [12].The digital CMS sequence is as follows. After the FD node is reset, the reset level is available in the column. The reset level is compared with the ramp voltage $V_{\rm ramp}$ generated by a D/A converter (DAC) and the BWI counter is set to count up synchronously. When $V_{\rm ramp}$ is equal to the reset level, the comparator output toggles from digital "high" to digital "low" and this stops the BWI counter from counting. The BWI counter value directly corresponds to the reset level in the column. For m-times sampling of the reset level, the reference ramp voltage $V_{\rm ramp}$ for the comparator will be up and down ramping for m-times, while the BWI counter will count m-times

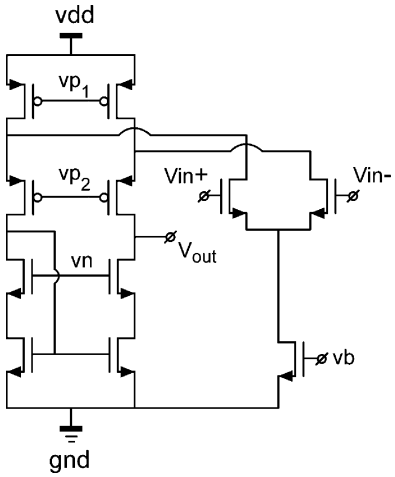

Fig. 2. Schematic of the folded-cascode column gain amplifier.

up. The latched counter output thus corresponds to m-times sampling of the reset level available on the column. After the signal charge from the photodiode is transferred to the FD node, V_C as the input voltage of the comparator goes up to the amplified signal level voltage accordingly. During the signal charge transferred from the photodiode to the FD node, every bit of the BWI counter is inverted to perform 1's complement operation by applying the control pulse B_1 and B_2. Then, after this inversion, the BWI counter will hold the negative digital value corresponding to the count of m-times pixel reset level sampling. From this negative digital value, the BWI counter then set to up counting for m-times again during pixel signal level sampling. The ramp voltage is configured in the same manner as in the case of the pixel reset level sampling. Eventually, the counters will digitally subtract the conversion of the sum of m-times sampling of reset signal from the sensor signal, and then do the averaging the output in digital domain. When m is 1, only the digital CDS is performed by the column readout chain.

The advantage of this CMS technique is the high thermal noise suppression capability in readout chain circuits which can be reduced by a factor of $\sqrt{m}$, where m is the number of samples. According to [8]–[10], the CMS technique is also useful in reducing the random telegraph signal (RTS) noise which is the dominating random noise source for noisy pixels in CIS, when a large number of m is applied. The RTS limits the imaging quality under low-light conditions for CIS in deep-submicron technologies [15], [16].

C. Column-Parallel Gain Amplifier

The column-parallel gain amplifier is used to amplify the voltage difference between its inverting and noninverting input nodes. Fig. 2 shows the schematic of the column-parallel gain amplifier used in Fig. 1(a), in which $\mathrm{Vin}+$ and $\mathrm{Vin}-$ are the noninverting and inverting input node, V_{out} is the output node, and vp_1, vp_2, vn, and vp are the bias signals of the amplifier, respectively. The amplifier is implemented using a folded-cascode architecture which gives high open-loop gain at 3.3 V power supply. The closed-loop gain of the amplifier is set by the ratio of the input capacitor C_{in} and the feedback capacitor C_{fb}, as shown in Fig. 1(a). The specifications and simulated performance of the column-parallel gain amplifier are summarized in Table I.

TABLE I
COLUMN-PARALLEL GAIN AMPLIFIER SPECIFICATIONS

Parameters	Value
Power Supply	3.3 V
Gain Stage	×2, ×4, ×8, ×12
Output Swing	1.35 V
Open loop Gain	81.6 dB
-3dB Bandwidth	3 Hz ~ 11 MHz (Gain=12)
Phase margin	>62.68°
SNR	65~70 dB
Total Noise	129 μV_{rms} (Gain=1)
Power Dissipation	0.39 mW
Settling time	<160 ns
Slew rate	>25 V/μs

III. NOISE ANALYSIS

The noise reduction effect by the proposed column readout chain is mainly coming from the column-parallel gain amplifier and subsequent digital CMS. To estimate the noise performance, after the reset noise and offset of each stage are cancelled, the thermal noise through the readout chain is analyzed as follows.

The total noise contributed by the pixel source follower usually has three main components: the thermal noise in the reset phase, the thermal noise in the amplification phase, and frequency related $1/\mathrm{f}$ and RTS noise. The thermal noise of the pixel source follower at the output of the column gain amplifier, $\overline{V_{\mathrm{ns}}^2}$, is given as [18]

$$\overline{V_{\mathrm{ns}}^2} = \frac{G^2 N_{\mathrm{sf}} \xi_{\mathrm{sf}} kT}{C_p + C_{\mathrm{in}}} + \frac{G^2 N_{\mathrm{sf}}^2 \xi_{\mathrm{sf}} kT}{g_{ms}} \omega_a \tag{1}$$

where G is the amplifier closed loop gain, defined by $C_{\mathrm{in}}/C_{\mathrm{fb}}$, k is Boltzman's constant, T is the absolute temperature, C_p is the column parasitic capacitor shown in Fig. 1(a), g_{ms} is the transconductance of the source follower, ω_a is the cutoff angular frequency of the column gain amplifier, and N_{sf}, ξ_{sf} are the noise gain factor and excess noise factor of the source follower, respectively [17], [18].

The first and second term of (1) represent the source follower thermal noise component in the reset phase and the amplification phase, respectively. During the reset phase, the column gain amplifier is in unity gain configuration mode, the first term in (1) represents the source follower thermal noise in this phase and sampled on the amplifier's input capacitor. The input capacitor of the amplifier consists of the input capacitor C_{in} and column parasitic capacitor [C_p as shown in Fig. 1(a)]. This thermal noise, which is also referred as the sample-and-transfer noise component in [7], is transferred to the feedback capacitor C_{fb} in the amplification phase and eventually sampled in the comparator auto-zero capacitor C_{az} in Fig. 1(a). Because this noise component stays unchanged during the amplification phase, it is

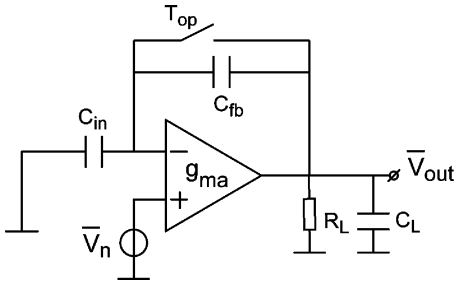

Fig. 3. Equivalent schematic diagram for column-parallel gain amplifier noise analysis in the amplification phase.

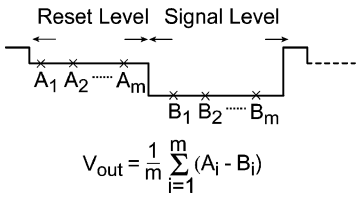

Fig. 4. Sampling diagram and the sensor output with CMS.

sampled as a fixed charge on the capacitor and can be cancelled by the digital CMS later.

Fig. 3 shows an equivalent schematic for deriving the noise of the column gain amplifier during the amplification phase. The noise of the column gain amplifier is represented as a noise voltage source at the input. The output noise of the column gain amplifier during amplification phase, $\overline{V_{\rm na}^2}$, is given as [6], [18]:

$$\overline{V_{\rm na}^2} = \frac{(1+G)^2 \xi_a kT}{g_m} \omega_a \tag{2}$$

where g_m and ξ_a are the transconductance and an excess noise factor of the gain amplifier, and ω_a is approximately equal to $g_m/[(1+G)C_L]$, in which C_L is the load capacitance of the gain amplifier.

Fig. 4 shows the sampling diagram and the sensor output using digital CMS. The thermal noise from the readout chain will be reduced by a factor of $1/\sqrt{m}$ using m-times digital CMS. Therefore, for $G \gg 1$, the resulting input-referred noise from the proposed readout chain with CMS, $\overline{V_n^2}$, is given as

$$\overline{V_n^2} = \frac{2}{m}\left(\frac{N_{\rm sf}^2 \xi_{\rm sf} kT g_m}{(1+G)\,{G_{\rm sf}}^2 C_L g_{ms}} + \frac{\xi_a kT}{(1+G)\,G_{\rm sf}^2 C_L} + \frac{\overline{V_{\rm no}^2}}{G^2}\right) \tag{3}$$

where $G_{\rm sf}$ is the gain of pixel source follower, and $\overline{V_{\rm no}^2}$ represents the other thermal noise source in the readout chain. Equation (3) shows the reduction of the input-referred thermal noise of the gain amplifier and the pixel source follower by a factor of $\sqrt{G}$, where G is the closed-loop gain of the column amplifier. The other thermal noise is reduced by a factor of G. By the CMS and averaging process, the overall thermal noise is further reduced by $\sqrt{m}$, where m is the number of sampling times.

IV. Measurement Results

A prototype test sensor with the proposed column-parallel readout circuits was designed and fabricated in a 0.18 μm 1-poly 4-metal CIS process from TSMC. The specifications of the test sensor are summarized in Table II. Fig. 5 shows the test chip microphotograph. To test the functionality and to better understand the proposed column parallel readout circuits, a small array of pixels was implemented, and due to the limited chip area and wire bonding conditions, the column gain amplifier array was implemented on the right side of the chip layout, rather than underneath the pixel array. The test setup for sensor's characterization includes a PCB board and a frame grabber board which is installed in a desktop computer. The sensor's output data is collected by the frame grabber board through the interconnector on PCB board, analyzed and recorded in real time by Labview for the measurements. The phase lock loop (PLL) and DAC circuits, needed to generate the ramp voltage, are implemented externally. The sensor's configuration timing is supplied by an external FPGA. The system clock frequency to drive the sensor is 10 MHz, and a 120 MHz clock is used to drive the column-parallel SS-ADC during the sensor performance characterization. By varying the configuration of the ramp voltage, the sensor can provide 10 or 12 bit output resolution.

TABLE II
The Prototype Test Chip Specifications Summary

Specification	Value
Process	TSMC 0.18μm 1p4m CIS
Chip Size	2.34mm (H) × 1.46mm (V)
Pixel Type	4T APS with pinned-photodiode
Pixel Size	10μm (H) × 10μm (V)
Number of Effective Pixels	7 (H) × 2 (V)
Power Supply	3.3V (A) / 1.8V (D)
Output	10/12 bit digital resolution
Column-parallel Amplifier Gain	×2, ×4, ×8, ×12
Digital CMS Mode	1, 2, 4, 8, 16 in 10bit resolution 1, 2, 4 in 12bit resolution

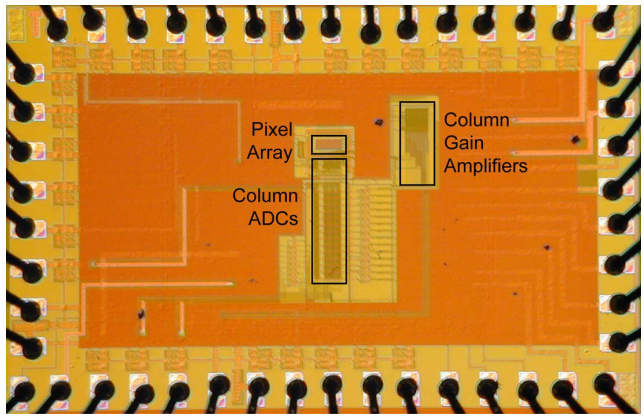

Fig. 5. Test chip microphotograph.

The 14 bit column-parallel SS-ADC has n-bit resolution margin for the m-times sampling of pixel outputs, where $n = \log_2 m$. A successive configuration of digital CMS with m-times sampling in k bit ADC resolution has a total equivalent data resolution of $k+n$ bits, where k is 10 or 12 for the test chip. Therefore, for the dark random noise characterization, the digital CMS is able to continue until 16 times sampling in 10 bit

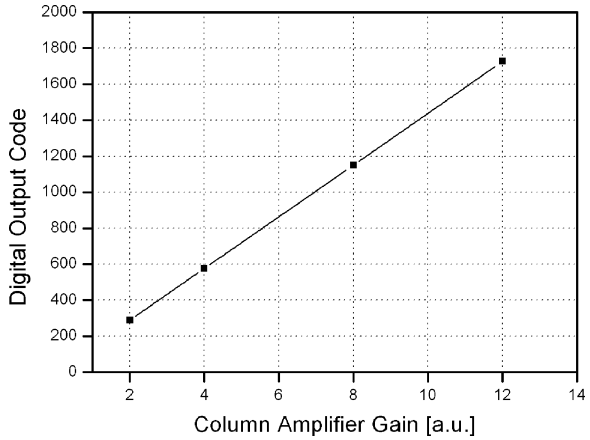

Fig. 6. Output characterization of the column readout chain.

ADC resolution mode, while the ADC is in 12 bit resolution mode, the digital CMS is continued until 4 times sampling.

Fig. 6 shows the output of the column readout chain with different column amplifier gain. The measurement is done with limited amount of light for the pixels to avoid saturation condition at the amplifier output in the column, and only the digital CDS, i.e., digital CMS with $m = 1$, is implemented. There are two types of gain error associated with the column gain amplifier: the gain amplification error and the gain deviation error among columns. The results show that the maximum gain error from the column gain amplification is about 0.8%, which is defined by the ratio of the measured amplified output codes over the ideal ones. The maximum column gain deviation error is about 5%, which is defined by the ratio of the output standard deviation among columns over their averaged values after amplification. The gain deviation errors within columns will cause a residual fixed pattern noise (FPN) on the column level. A column-based digital correction technique proposed in [4] and [5] can be useful to reduce the effects of column FPN.

Fig. 7(a) and (b) show the measured differential nonlinearity (DNL) and integral nonlinearity (INL) plot of the column-parallel SS-ADC. The histogram test approach [14] is used to measure the nonlinearity of the SS-ADC. A 1.5 Hz sinusoidal wave signal is applied to the ADC after low-pass filtering. From the measured results, the worst DNL is within $-0.8/+0.6$ least significant bit (LSB) and the worst INL is within $-2.0/+4.0$ LSB, which corresponds to a 0.58% nonlinearity. The nonlinearity of the ADC is well below the nonlinearity of the pixel (pinned-photodiode and source follower) which is at least 1% and thus can be neglected [20]. The parasitic capacitance from the input to the output of the comparator can be the probable cause of this nonlinearity, and it can be further improved by the layout optimizations.

Fig. 8 shows the measured random noise of the sensor versus the column amplifier gain in 12 bit ADC resolution. Only digital CDS ($m = 1$) is applied for this measurement. It is shown that when the column amplifier gain G is increased, the noise is first decreasing by a factor of G and then by a factor of $\sqrt{G}$, which is corresponding to the tendency indicated by (3).

Fig. 9(a) and (b) show the input referred dark random noise measurement results of the test sensor in 10 bit and 12 bit ADC

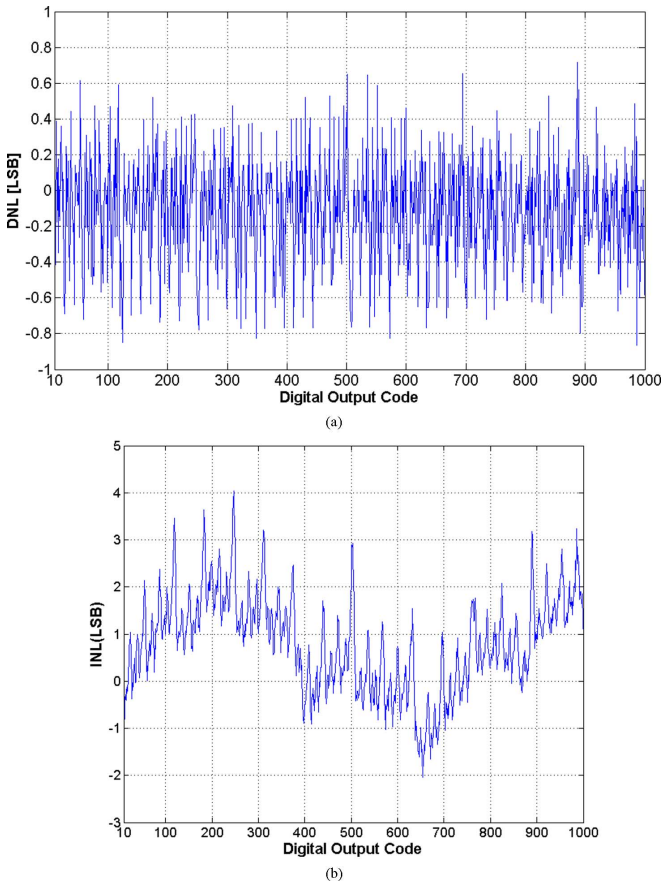

Fig. 7. Measured column ADC nonlinearity: (a) DNL and (b) INL in 10 b resolution mode.

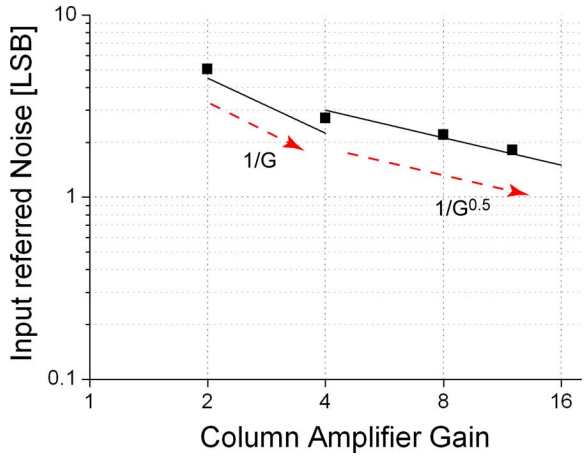

Fig. 8. Measured random noise versus the column amplifier gain.

resolution mode. While in 10 bit ADC resolution, the complete configuration time from pixels to the column readout chain is 5.7 μs for digital CDS, and it up to 65 μs for 16 times digital CMS. While in 12 bit ADC resolution mode, it is 23.8 μs for digital CDS, and then up to 62 μs for 4 times digital CMS. The dark random noise reduction of the proposed readout chain with digital CMS is about 70% in 10 bit ADC resolution mode where the gain of column amplifier is 12 and with 16 times digital CMS. This noise reduction will gain 10.4 dB increase of SNR. And the dark random noise reduction is about 50% where the

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART

Reference	Technology	ADC Type	ADC Resolution	Conversion Gain [μV/e⁻]	Random Noise [μV_{rms}]
[2]	0.13-μm CMOS	SAR	14b	45	131 (analog gain ×8)
[21]	0.13-μm CMOS	ΔΣ	13b	80	152
[22]	0.18-μm CMOS	Cyclic	13b	61	299
[23]	0.18-μm CMOS	Folding integration/Cyclic	13b-19b	67	80
[12]	0.18-μm CMOS	SS	10/12b	40	284
[11]	90-nm CMOS	SS	10/12b	110	121 (analog gain ×16)
[24]	0.35-μm CMOS	MRSS	10b	46	490
This work	**0.18-μm CMOS**	**SS**	**10/12b**	**45**	**127 (analog gain ×12)**

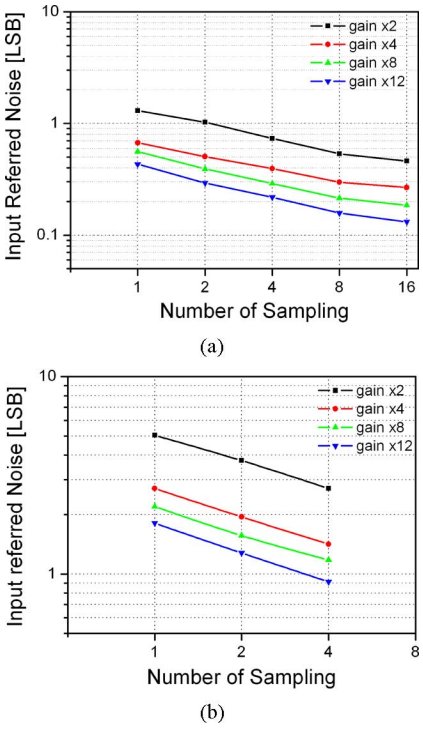

Fig. 9. Measured input referred dark random noise of the sensor in: (a) 10 bit and (b) 12 bit ADC resolution mode.

gain of column amplifier is 12 and with 4 times digital CMS. This noise reduction will gain 6 dB increase of SNR. The input referred dark random noise is 127 $\mu V_{\rm rms}$ at the column amplifier gain of 12 with 16 times digital CMS in 10 bit ADC resolution mode, and 219 $\mu V_{\rm rms}$ at the column amplifier gain of 12 with 4 times digital CMS in 12 bit ADC resolution mode. It is also referred that the noise reduction effect of digital CMS will be limited by the noise in frequency domain, i.e., $1/f$ noise from the pixel source follower, as the number of sampling times is increasing.

A comparison of this work with the state-of-the-art is listed in Table III. As shown, compared with [11], [12], and [24], this work achieves the state-of-the-art performance in random noise level.

V. CONCLUSION

A prototype CMOS image sensor with a new type of column readout chain is presented. The test sensor achieves a low-noise performance by using the column-parallel gain amplifier together with a digital CMS algorithm. Different with the other approaches to implement a CMS technique such as the FI-CMS technique in [10], our proposed design does not need extra circuits in the columns. Because the CMS technique in our design is configured in the digital domain, it makes the sensor readout scheme very straightforward, and also compared with [10] and [23], the architectural simplicity of our proposed circuits makes it much easier to implement the design and adapt it to other process technologies. The measurement results show that the proposed column-parallel circuits achieve about 0.8% gain amplification error and 0.58% nonlinearity. Due to a limited chip area, a large amount of pixels for the noise characterization with detailed information is not available with this prototype test sensor. However, with quite a few number of pixels, the dark random noise measurement results still show that the use of the proposed column-parallel circuit with digital CMS technique is able to achieve a drastically reduction of the random noise, i.e., nearly 70% reduction. This is an attractive benefit to use this proposed column-parallel circuit to enhance the SNR of imagers with 10.4 dB for low-light imaging application. For further improvement of using the proposed column-parallel circuit with a large amount of pixels, certain column-based digital correction techniques proposed in [4] and [5] or off-chip FPN cancellation techniques are helpful to deal with the extra residual column level FPN introduced by the high-gain column amplifier.

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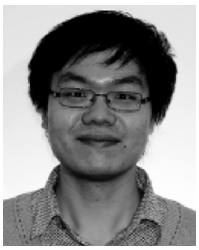

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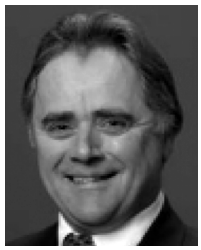

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