A Potential-Based Characterization of the Transfer Gate in CMOS Image Sensors

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***Abstract*— A method to characterize the transfer gate (TG)-related parameters in a 4 T pixel is presented. The method is based on the pinning voltage measurement, which is proposed by Tan *et al.* [1] Using this method, the TG ON and OFF surface potential can be characterized. Based on the TG ON potential characterization, and according to the MOSFET model, the TG channel doping and the oxide thickness can be extracted from the measurements. Based on the TG OFF potential characterization, the TG surface potential dependence on the TG design parameters and the pixel biasing condition are analyzed. Using this method, whether the device is suffering from the drain-introduced barrier lowering effect or the short channel effect can be easily determined.**

***Index Terms*— CMOS image sensor (CIS), full well capacity (FWC), pinning voltage, potential barrier, transfer gate (TG).**

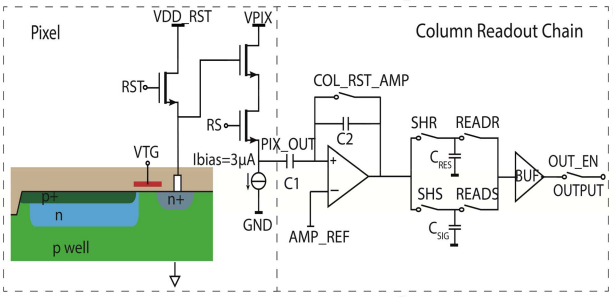

Fig. 1. Simplified schematic of a 4 T nMOS pixel and the column readout chain, including a column gain amplifier, a sample and hold circuit, and a column buffer.

I. Introduction

NOWADAYS the pinned photodiode-transfer gate-floating diffusion (PPD-TG-FD) structure is the preferred choice for most pixel designs. The advantages of this structure include low noise, high quantum efficiency, and low dark current [2].

Recently, based on the pinning voltage measurement [1], two intensive studies [3], [4] have been presented to characterize the PPD-TG-FD structures. A few parameters, such as the PPD capacitance, pixel equilibrium full well capacity (EFWC), and TG threshold voltage, are extracted. However, these studies mainly focus on the PPD characterization. In this paper, the focus is on the TG characterization. The TG design and the technology are important for pixel performance. However, the method of the TG characterization is not straightforward. In this paper, the surface potential-based TG analysis and characterization is given. A method to characterize the TG ON and OFF surface potential is developed. To understand the TG behavior for different technologies and designs, we have implemented two test chips. These two test chips (chips A and B) used two different fabrication technologies (processes A and B).

To characterize the different states of the TG, four different regions are proposed in this paper. The under-gate surface potential on both the TG OFF and on states can be characterized based on these four regions.

For the TG ON-state characterization, inspired by [3], a MOSFET classic model is applied to analyze the PPD-TG-FD states by means of the pinning voltage measurement. In [3], a solution is proposed to extract the channel doping concentration. Compared with [3], based on the similar theoretical model, this paper proposes a different extraction method from the measurement results. Using our extracted process parameters, the applied MOS model achieves better agreement with the measurement results compared with [3].

For the TG OFF-state characterization, the TG potential barrier can be measured. The dependence of the TG OFF potential barrier on the TG design parameters and the pixel biasing condition will be investigated by means of the measurement results of different pixel design parameter variations. According to the proposed characterization method, it is easy to determine whether the TG design is suffering from short channel effect and/or drain-induced barrier lowering (DIBL) effect.

II. Test Pixel and Measurement

For the pixel characterization, a test image sensor chip with 80 different pixels was implemented. A similar sensor design was implemented in two distinct technologies. Both of these technologies (process A and process B) are commercial 0.18-μm PPD CMOS image sensor processes. Fig. 1 shows the implemented test pixel cross section and the column readout chain schematics. The source follower biasing current is set to 3 μA. There are a few different PPD length (PPL) and width (PPW) and TG length (TGL) and width (TGW) variations included in the designs. The timing diagram for the PPD parameter extraction is illustrated

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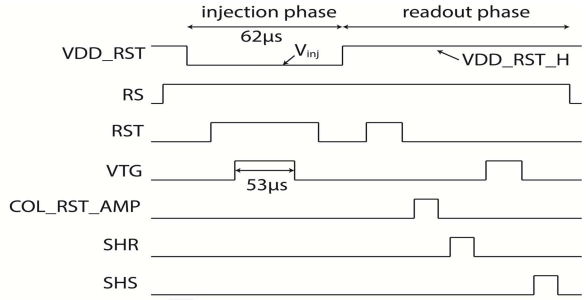

Fig. 2. Timing diagram of the pinning voltage measurement. Compared with the normal pixel readout, the node VDD_RST is changed to a pulse. Both the high voltage (VDD_RST_H) and the low voltage levels (V_{inj}) can be adjusted externally.

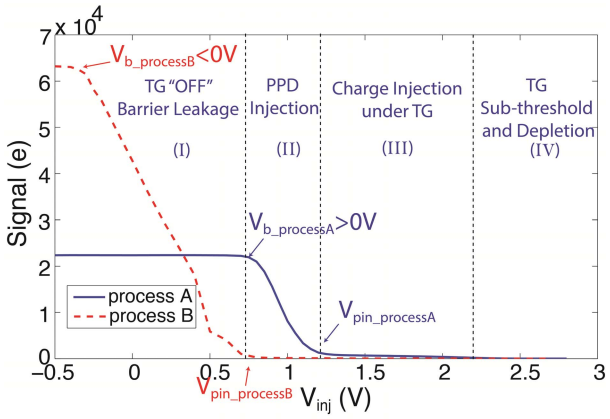

Fig. 3. Pinning voltage measurements (for processes A and B) can be divided into four regions. (I) TG OFF barrier leakage. (II) PPD injection. (III) Charge injection under TG. (IV) TG subthreshold and depletion.

in Fig. 2. This measurement can be divided into two phases: 1) the injection and 2) the readout phases. In the injection phase, the node VDD_RST is biased to a relatively low voltage (V_{inj}). This voltage defines the injection potential for the PPD and the FD node. To inject electrons into the FD node and PPD, both the RST and the TG are switched to the ON state. The injection phase and the TG pulse should be kept long enough to ensure the whole PPD potential is biased as injection voltage [3]. Here, a 53-μs TG injection pulse is used, which is long enough. After the injection, the TG is closed to keep the injected electrons stored in the PPD. The readout phase takes place like a normal imaging readout, where the VDD_RST is changed to a high voltage level. The reset transistor RST is switched on again to reset/empty the FD node. After the reset level sampling on the capacitance C_{RES}, the TG is opened. The stored electrons transferred and stored on the capacitance C_{SIG}. The measurement needs to take place multiple times while varying V_{inj}.

III. Transfer Gate Characterization

A. Characterization Description

With an increasing injection voltage, a few potential steps in the PPD-TG-FD structure can be characterized. Fig. 3 plots two similar pixel pinning voltage measurements resulting

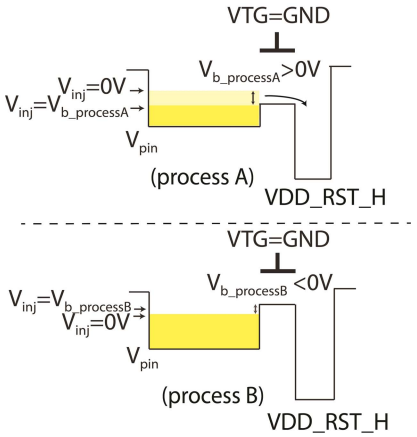

Fig. 4. Potential diagram analysis for processes A and B. The injected electrons at a potential higher than the TG OFF potential barrier will overflow to the FD node when the FD node is reset to a high voltage VDD_RST_H.

from the two different processes. Based on the output signal-changing trend, the curve can be divided into four different regions. The four region divisions are shown in Fig. 3 based on the measurement result of process A.

For the curve of process A, the signal readout from the PPD is constant when V_{inj} is small. Increasing the injection voltage until $V_{\text{inj}} = V_{\text{b\_process A}}$ (the first keen point of the curve), the output begin to decrease with the V_{inj} increasing further. This means when $V_{\text{inj}} < V_{\text{b\_process A}}$, the output signal is saturated by the readout out chain, FD node, or TG OFF potential barrier. In our case, since the same FD node and readout chain can achieve a larger readout signal level for a larger PPD, the limitation is the TG OFF potential barrier. This flat part is the TG OFF barrier leakage region. When the injection phase is changed to the readout phase, the number of electrons held in the PPD will be readout. If the TG cannot produce a sufficiently high barrier (when TG is OFF) to prevent an overflow of charge, part of the electrons held in the PPD will be lost during the FD node reset. The voltage of the TG potential barrier can be characterized as $V_{\text{b\_process A}}$, which can be extracted from the first knee point of the measurement curve. V_b is defined as the potential difference between the lowest potential of the barrier beneath the TG (when TG is OFF) and the PPD electron potential in equilibrium state ($V_{\text{inj}} = 0$ V). In this region ($V_{\text{inj}} < V_{\text{b\_process A}}$), with the increasing injection voltage from 0 V to V_b, fewer electrons are injected into the PPD. Even with fewer injected electrons, the readout electrons are constant. The potential barrier limits the number of electrons, which can be held. When the TG OFF barrier is equal to V_{inj}, no more electrons are lost during the FD node reset. The top diagram in Fig. 4 (process A) also illustrates this situation.

The measurement result of process B looks similar to the result shown in [3]: $V_{\text{b\_process B}} \approx -0.4$ V. When $V_{\text{inj}} < 0$ V, the PPD is forward biased. The forward current of the PPD [5] could influence the FWC of the PPD. In the real operation condition, the FWC is highly depend on the photon flux [5]–[7]. Thus, the measured $V_{\text{b\_process B}}$ gives an estimation of real V_b, which is also related to the photon flux. The bottom diagram in Fig. 4 (process B) illustrates

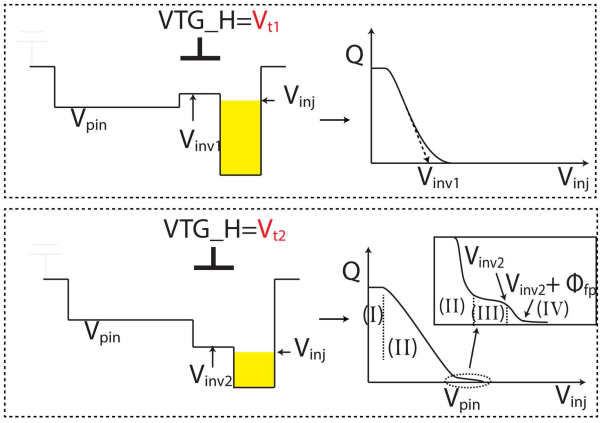

Fig. 5. Left: potential diagrams under different TG high voltages. Right: corresponding measurement results. $V_{t1} < V_{t2}$; $V_{\text{inv1}} < V_{\text{pin}} < V_{\text{inv2}}$.

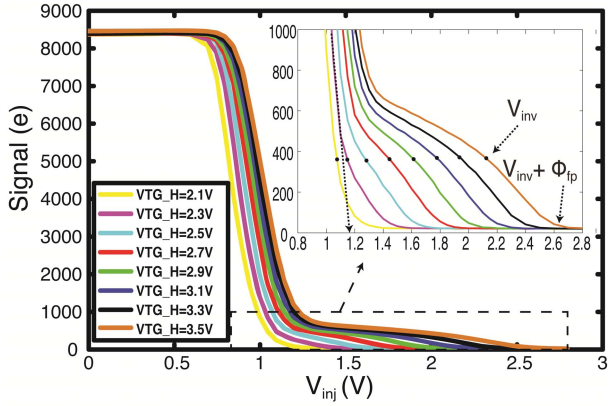

Fig. 6. Same pixel (PPL = 3.2 μm, PPW = 4 μm, TGL = 0.6 μm, and TGW = 4 μm) under different TG high voltages measurement results. Based on these results, V_{inv} and ϕ_{fp} are extracted.

the situation. A larger V_b means a lower TG OFF barrier potential, more leakage of electrons to the FD node and a lower FWC in the PPD. Except for the specific values of parameters, e.g., V_b and V_{pin} (the pinning voltage of PPD [1], [8]), the two measurement curves shown in Fig. 3 have a similar shape. The working principle of the pixels and their physical models should also be the same.

With a further increase in the injection voltage, when $V_b < V_{\text{inj}} < V_{\text{pin}}$, the measurement characterizes the PPD injection region. In this region, all the injected electrons in the PPD can be recollected by the signal readout. No overflown electrons are lost during the FD node reset operation. The number of injected electrons in the PPD is reduced with an increase in the injection voltage (V_{inj}).

When $V_{\text{inj}} = V_{\text{pin}}$, the entire PPD structure is depleted. The potential difference between the p-well and n-well doping in the PPD structure cannot be enlarged. No electrons can be directly injected into the PPD structure. However, if the TG voltage is high enough, the charge will be injected underneath the TG [9] and then kicked back [3], [10] into the PPD during the TG ON–OFF transition period. The number of kicked-back charges is very limited compared with the PPD injection region.

Before the TG is completely depleted, there is also a subthreshold part, resulting in fewer electrons being injected under the TG. The injection voltage is increased until the TG is fully depleted, at which point no electrons can be injected under the TG. The region is defined as the TG subthreshold and depletion regions.

The division point between the PPD injection region and the TG subthreshold and depletion regions is the TG threshold inversion point. The corresponding injection voltage is defined as V_{inv}. In Fig. 5, there are two situations given for the TG high voltage. When the TG high voltage is equal to V_{t1} [Fig. 5 (top)], the corresponding injection voltage, which makes the TG turn into the inversion point, will be V_{inv1}. If $V_{\text{inv1}} < V_{\text{pin}}$, with the increase in V_{inj}, the number of output electrons will be decreased until V_{inj} reaches V_{inv1}. The charge injection on the TG region will disappear and V_{pin} cannot be extracted from the measurement. If the TG voltage is high enough, like VTG_H $= V_{t2}$ [Fig. 5 (bottom)], V_{inv2} and V_{pin} will differ slightly. The corresponding injection voltage, which turns the TG into the inversion point, will be V_{inv2}. If $V_{\text{inv2}} > V_{\text{pin}}$, we can extract both V_{pin} and V_{inv2}. Because the injection current is saturated in the strong inversion region, the surface potential of the channel is also nearly constant. A further increase in the injection voltage will cause the TG state to change into the weak inversion until $V_{\text{inv2}} + \phi_{\text{fp}}$. ϕ_{fp} is the difference (in volts) between the intrinsic Fermi level and the Fermi level of the silicon under the TG. With a further increase in V_{inj} from $V_{\text{inv2}} + \phi_{\text{fp}}$, the TG region will be depleted, and no electrons can be injected under the TG.

All in all, the TG OFF barrier leakage region is determined by how many electrons can be held in the PPD, i.e., by the TG OFF potential barrier. Thus, from this region, the TG OFF potential barrier can be extracted. The other three regions are determined by how many electrons can be injected from the FD node into the PPD and under the TG, which happens during the injection phase of the measurement. From the charge injection under TG and TG subthreshold and depletion regions, the TG ON state can be characterized.

B. Transfer Gate Parameter Extraction

Based on the analysis of the TG subthreshold and depletion regions above, V_{inv} and $V_{\text{inv}} + \phi_{\text{fp}}$ can be found from the measurement result if the TG high voltage is high enough that ($V_{\text{inv}} > V_{\text{pin}}$). Fig. 6 shows the process A measurement results for different TG high voltages, ranging from 2.1 to 3.5 V. The different TG high voltages correspond to different inversion voltages V_{inv}. These different values of V_{inv} can be extracted from Fig. 6. For large TG voltages (here VTG_H > 2.9 V), V_{inv} and $V_{\text{inv}} + \phi_{\text{fp}}$ are easier to identify. The voltage difference ϕ_{fp} can be calculated from both the inversion point (V_{inv}) and the subthreshold point $V_{\text{inv}} + \phi_{\text{fp}}$ in the plot. Here, ϕ_{fp} is about 0.45 V. Therefore, the doping concentration N_a is equal to 5.5×10^{17} cm^{-3}, as can be

calculated from

$$\phi_{\mathrm{fp}} = \frac{kT}{q} \ln \frac{N_a}{n_i}. \tag{1}$$

The extracted ϕ_{fp} value has been approved by different pixel design measurements. This value is not influenced by the design, but only by the process. However, the existence of region (III) is one condition to accurately extract ϕ_{fp}. To further verify the proposed extraction method, VTG_H and the channel surface potential relationship, which is similar to the extraction method mentioned in [3], can be used for verification.

The PPD-TG-FD structure has been seen as a special MOS transistor. According to the law of conservation of potential energy and charge, for an MOS transistor, the following formula can be written [11]:

$$V_G = \frac{(2q\varepsilon_{\mathrm{si}}N_a)^{\frac{1}{2}}}{C_{\mathrm{ox}}}\phi_s^{\frac{1}{2}} + V_{\mathrm{FB}} + \phi_s \tag{2}$$

where V_G is the applied gate voltage, ϕ_s is the surface potential of silicon under the TG, and V_{FB} is the flat band voltage $V_{\mathrm{FB}} = \phi_{\mathrm{ms}} - (Q'_{\mathrm{ss}}/C_{\mathrm{ox}}) \approx -(E_g/2) - \phi_{\mathrm{fp}}$. ϕ_{ms} is the work function difference of the polymetal–semiconductor. Suppose that the n^+ poly is used as the metal. Q'_{ss}, which is the charge in the oxide per unit area, has been neglected; here, the inversion layer charge is also neglected before the strong inversion, because it is quite small compared with the charge in the depletion region. Equation (2) is valid before the threshold inversion point. Thus, the inversion condition will be the boundary condition of (2). Due to the injection voltage (V_{inj}) applied to the source (FD), and considering the substrate bias effect, the inversion condition is

$$\phi_s = 2\phi_{\mathrm{fp}} + V_{\mathrm{inv}}. \tag{3}$$

Furthermore, in the strong inversion situation, the surface potential will stay pinned to $2\phi_{\mathrm{fp}} + V_{\mathrm{inv}}$ varying only logarithmically [12]. Combine (2) and boundary condition (3), in threshold inversion point, the relationship between gate voltage and V_{inv} can be derived

$$V_{\mathrm{th}} = \frac{(2q\varepsilon_{\mathrm{si}}N_a)^{\frac{1}{2}}}{C_{\mathrm{ox}}}(V_{\mathrm{inv}} + 2\phi_{\mathrm{fp}})^{\frac{1}{2}} + V_{\mathrm{FB}} + V_{\mathrm{inv}} + \phi_{\mathrm{fp}}. \tag{4}$$

The work in [3] used the same relationship (4) between V_{inv} and VTG_H to extract the channel doping concentration (N_a). However, in this formula, there are two unknown parameters (N_a and C_{ox}). Thus, based on (4), extracting N_a in [3] still needs an extra C_{ox} value. Furthermore, according to our analysis, the V_{inv} extraction method in [3] is not accurate enough; the extraction result cannot fully fit the measurement point. To improve the extraction method, in this paper, N_a has been found by ϕ_{fp} extraction in Fig. 6. Using the calculated value ($N_a = 5.5 \times 10^{17}$ cm^{-3}) and formula (2), the thickness of gate oxide $t_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/C_{\mathrm{ox}}$ can be derived.

The V_{inv} extraction method has been introduced in Section III-A. Moreover, at the inversion point and for the same pixel, the number of electrons injected under the TG will be the same for different TG voltages. Based on the extraction result of V_{inv} from the measurement result shown in Fig. 6 and inversion conditions (3), the relationship between ϕ_s and VTG_H is plotted in Fig. 7. This relationship should also fit (2). Using all these extracted process parameters, and according to (4), the $t_{\mathrm{ox}} = 70$ nm is derived and the threshold voltage $V_{\mathrm{to}} \approx 0.85$ V ($V_{\mathrm{inj}} = 0$ V) can be derived. The measurement points can fit the extracted value perfectly. The extracted parameter t_{ox} is also consistent with the information provided by the foundry, which proves the validation of the proposed TG parameter extraction method for process A.

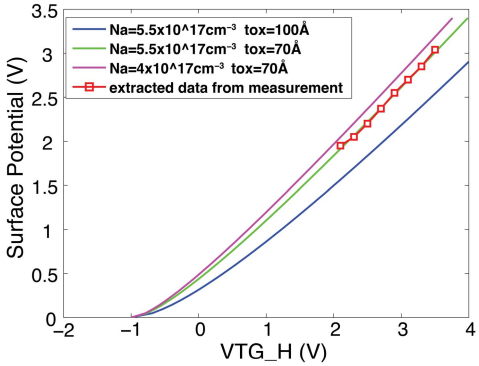

Fig. 7. TG high voltage versus the corresponding extracted surface potential from the measurement result for processing parameters fitting.

IV. Transfer Gate OFF Potential Barrier Dependence

According to the discussion in Section III-B, the parameter V_b can be extracted from the pinning voltage measurements, which can be used to characterize the TG OFF potential barrier. From a few different pixel design measurements, the TG OFF potential barrier dependence has been investigated based on process A. Besides the technology parameters, there are other parameters and secondary order effects that can influence the TG OFF potential barrier, thus influencing the full well capacitance of the photodiode as well.

Lowering the TG low voltage can increase the TG potential barrier and further increase the FWC [13]. The measurement result shown in Fig. 8 also proves this. The two curves in Fig. 8(a) compare VDD_RST_H = 2.3 and 3.3 V, which also proves the influence of the DIBL effect.

A. Drain-Induced Barrier Lowering Effect

During the image sensor operation, in order to readout out the electrons, the FD node has to be reset to a high voltage (VDD_RST_H) before the charge transfer takes place. In addition, the direction of the electron movement in the readout phase will be from the PPD to the FD node. Therefore, in this phase, the FD node can function as the drain of the MOSFET. In a MOSFET, the drain potential can also influence the gate barrier potential in certain circumstance, which is known as the DIBL effect. Similarly, VDD_RST_H applied on the FD node will partly control the TG OFF potential barrier.

DIBL is a mechanism to describe a drain bias, which causes a lowering of the source channel junction barrier [14]. This effect occurs in short channel devices. When the

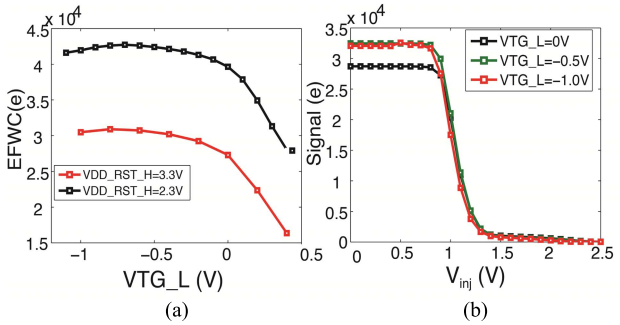

Fig. 8. (a) EFWC [3] increase with a decrease in the TG low voltage (VTG_L) ($V_{\text{inj}} = 0$). (b) Pinning voltage measurements under three different VTG_L values. Decreasing the value of VTG_L improves the potential barrier height (V_b decrease) (PPL = 3.2 μm, PPW = 12 μm, TGL = 0.6 μm, and TGW = 6 μm).

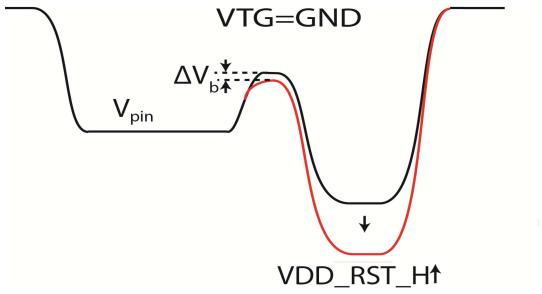

Fig. 9. Potential diagram shows due to the DIBL effect, under the same short TGL situation, increasing the FD node reset voltage could lower the TG OFF potential barrier.

TGL reduces and VDD_RST_H increases, the depletion region of the FD node moves closer to the depletion region of the PPD. The two electric fields will interact with each other, and the charge can no longer be regulated only by the VTG. In the most extreme situation of DIBL, the two depletion regions touch each other, creating a conduction path without any influence of the gate bias. Fig. 9 shows the DIBL effect potential diagram. Increasing the high reset voltage (VDD_RST_H) will increase the space charge region of the TG-FD junction, which will decrease the potential barrier for a short TG pixel. Finally, the FWC will be decreased due to the DIBL effect. It is worth mentioning that normally, without considering the DIBL effect, increasing the reset voltage can increase the FWC by increasing the voltage swing of the FD node. However, if the FD node capacity is large enough for the PPD size, but the TGL is not long enough, the FWC will be determined by the PPD size, pinning voltage, and potential barrier. Increasing the reset voltage will decrease the FWC due to the DIBL effect. The measurement results shown in Fig. 10 also prove this. For the same pixel (with a relatively low TGL of 0.52 μm), the potential barrier and the EFWC can be increased with a decrease in the FD node reset voltage. The potential barrier increase is indicated by a decrease in V_b (ΔV_b) in Fig. 10.

B. Short Transfer Gate Effect

As stated in the section on the DIBL effect, the short TG can cause the DIBL effect.

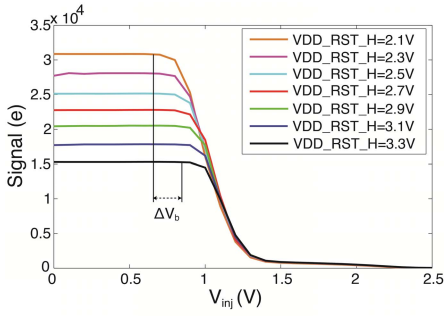

Fig. 10. Different reset voltage pinning voltage measurements for the DIBL effect (PPL = 3.2 μm, PPW = 12 μm, TGL = 0.52 μm, and TGW = 6 μm).

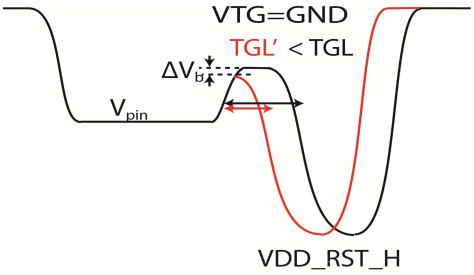

Fig. 11. Potential barrier influenced by the TGL due to the short channel effect.

In the ideal situation, it is assumed that the entire gate area will determine the length of the voltage barrier under the TG. However, in reality, since the space charge area of the PPD-TG and FD-TG will extend into the channel region, the effective channel length will be smaller than the designed one. For a long TG situation, the junction extension effect does not have much influence. However, for a short TG design, the gate control over the channel potential can vanish and result in punch-through under the TG. Fig. 11 plots the potential diagram of the PPD-TG-FD structure for the short TGL' and long TGL, which also shows a different potential barrier height for both the cases. Fig. 12 presents the pinning voltage measurement results for the same PPD size, high reset voltage, high and low TG voltages, but different TGLs. The results show that the V_b is decreased with an increase in the TGL. In Fig. 12, for the pixel lengths TGL = 0.8 μm and TGL = 1 μm, the V_b extraction and the PPD EFWC are limited by the FD node or readout chain. The real V_b is smaller than the point shown in this plot.

C. Narrow Transfer Gate Effect

Fig. 13 shows the cross section of the TG structure widthwise. In the ideal situation, the charge in the depletion region is $Q_{\text{SD}} = qN_a x_{dt}\text{WL}$ (x_{dt} is the width of the depletion region, and W and L are the gate width and length). Nevertheless, the actual depletion region in the channel is always larger than what is usually assumed for a 1-D analysis; this is due to the existence of fringing fields [15]. The extra charge introduced in the depletion region is ΔQ_{SD}, which can be calculated as [16]

$$\Delta Q_{\text{SD}} = qN_a L x_{dt}(\xi x_{dt})$$
$$Q_{\text{SD}} = qN_a x_{dt}\text{WL} + \Delta Q_{\text{SD}} = qN_a x_{\text{dt}}\text{WL}\left(1+\frac{\xi x_{dt}}{W}\right) \quad (5)$$

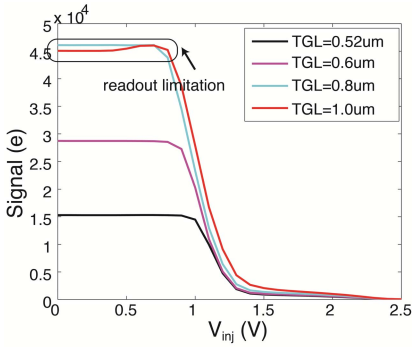

Fig. 12. Measurement results for pixels (PPL = 3.2 μm, PPW = 12 μm, and TGW = 6 μm) with different TGLs.

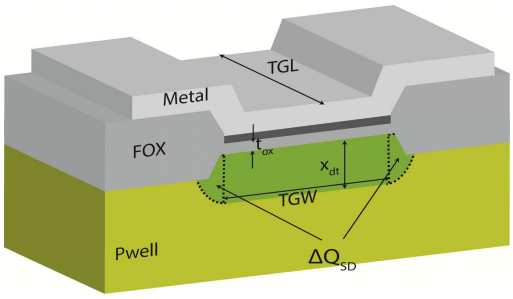

Fig. 13. Cross section of the TGW-wise direction indicating the extension of the two extra depletion regions from the gate.

where ξ is the parameter for the extension region. Suppose the total shape of the extension parts is the half round, then $\xi = 2/\pi$. The extensions of the two extra depletion regions for the field oxide also contribute to the charge required for the compensation of the TG voltage. If the TGW is big enough, the extra depletion regions can be neglected compared with the depletion region under the gate. However, with the decrease in the TGW, these depletion region extensions cannot be neglected anymore. Here, the extra depletion region charges introduced by the overlap between the TG and p+ layer of the PPD are neglected. Since this charge component is also proportional to W, the conclusion will not be changed.

Calculating the potential barriers introduced by different TGWs should result in finding the surface potential for the zero gate voltage $\Delta\phi_{s0}$. Here, VTG is constantly grounded. For TGW1 > TGW2, based on (2), the following formulas are valid:

$$\text{TGW1:}\ \phi_{S0\_\text{TGW1}} + V_{\text{FB}} + \frac{qN_a x_{dt1}}{C_{\text{ox}}}\left(1 + \frac{\xi x_{dt1}}{\text{TGW1}}\right) = 0 \tag{6}$$

$$\text{TGW2:}\ \phi_{S0\_\text{TGW2}} + V_{\text{FB}} + \frac{qN_a x_{dt2}}{C_{\text{ox}}}\left(1 + \frac{\xi x_{dt2}}{\text{TGW2}}\right) = 0 \tag{7}$$

$$x_{dt1} = \left(\frac{2\varepsilon_s \phi_{S0\_\text{TGW1}}}{qN_a}\right)^{\frac{1}{2}}$$
$$x_{dt2} = \left(\frac{2\varepsilon_s \phi_{S0\_\text{TGW2}}}{qN_a}\right)^{\frac{1}{2}}. \tag{8}$$

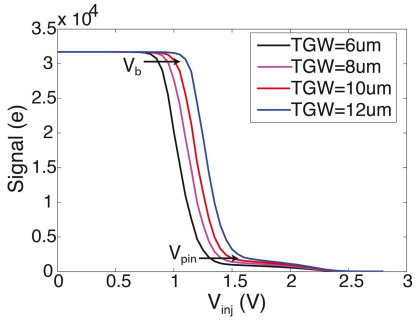

Fig. 14. Pinning voltage measurement for different transfer gate width (PPL = 3.2 μm and PPW = 12 μm, TGL = 0.6 μm). Both V_b and V_{pin} will be influenced by the TG width.

Substitute (8) [16] into (6) and (7), and comparing these two equations, it can be derived that

$$\left(1 + \frac{2\varepsilon_s \xi}{C_{\text{ox}}\text{TGW1}}\right)\phi_{S0\_\text{TGW1}} + \frac{(2qN_a\varepsilon_s)^{\frac{1}{2}}}{C_{\text{ox}}}\phi_{S0\_\text{TGW1}}^{\frac{1}{2}}$$
$$= \left(1 + \frac{2\varepsilon_s \xi}{C_{\text{ox}}\text{TGW2}}\right)\phi_{S0\_\text{TGW2}} + \frac{(2qN_a\varepsilon_s)^{\frac{1}{2}}}{C_{\text{ox}}}\phi_{S0\_\text{TGW2}}^{\frac{1}{2}}. \tag{9}$$

For TGW1 > TGW2, we can derive

$$\phi_{S0\_\text{TGW1}} > \phi_{S0\_\text{TGW2}}. \tag{10}$$

What this means is that if the TGW is decreased, then the TG OFF surface potential ϕ_{S0} will also be decreased. A smaller ϕ_{S0} means an almost flat band state and a higher potential barrier. Fig. 14 is the pinning voltage measurement for a few different pixels. These pixels have the same photodiode size (PPL = 3.2 μm and PPW = 12 μm) and the same TGL of 0.6 μm, and the same operation voltage (3.3V) applied for VTG_H and VDD_RST_H. However, they have a different TGW and FD size. A narrow TG corresponds to a smaller FD area. Based on the measurement result shown in Fig. 14, V_b is increased from about 0.8 to 1.2 V with the TGW increasing from 6 to 12 μm. This reveals that the potential barrier height is decreased about 0.4 V, which is consistent with the analysis above. It is worth mentioning that normally if the barrier height is increased, the FWC will also increase. However, from the measurement results here, we found that a narrow TGW also corresponds to a lower measured pinning voltage. Consequently, the FWC cannot be improved by decreasing the TGW.

In general, but depending on design and technology, the FD node reset voltage (VDD_RST_H), TGL, and TGW will also limit or regulate the potential barrier height of the TG OFF state. With the fully understanding of these mechanisms and effects, the designer can easily detect whether the FWC is limited by the short gate effect. The process and the pixel design can be optimized further to achieve better performances. To optimize the pixel design and to deal with the DIBL effect and short TG effect in the future work, we can use, for instance, a T-shaped TG, which can tradeoff the FWC and the charge transfer [17]. It is worth mentioning that the DIBL and the short gate effects are not universal for all the processes. The test chip B, which we also characterized, did not show these effects.

V. Conclusion

In this paper, using the measurement proposed in [1], a potential-based TG characterization is reported based on a particular process case. The surface potential under the TG will affect the charge transfer process. The doping concentration underneath the TG and the TG oxide thickness can be extracted from the measurement. When the TG is OFF, the potential barrier under the TG will modulate the FWC of the PPD. The FD node reset voltage TGL and TGW can have an influence on the TG OFF potential barrier under certain design and process conditions. An optimization of the potential barrier and the FWC can be realized based on the analysis and measurement results.

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